EXHIBIT 1

ASSERTED CLAIMS OF THE FAMILY 3 PATENTS

(1) Claim 5 of the U.S. Pat. No. 7,836,381 (as corrected on February 8, 2011):

[Preamble] A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

[a] transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

[b] determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

[c] allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

[d] allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and

[e] deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

Ex. 4 to Targowska Decl. (Bates Nos. TQD000221 – TQD000232).

(2) Claim 13 of the U.S. Pat. No. 7,844,882 (as corrected on May 3, 2011):

[Preamble] A system that allocates shared memory comprising:

[a] a transceiver that performs:

[a][1] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

[a][2] determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

[a][3] allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

[a][4] allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate; and

[a][5] deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

Ex. 3 to Targowska Decl. (Bates Nos. TQD000233 – TQD000244).

(3) Claim 1 of the U.S. Pat. No. 8,276,048:

[Preamble] A system that allocates shared memory comprising:

[a] a transceiver that is capable of:

[a][1] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

[a][2] determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

[a][3] allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

[a][4] allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

[a][5] interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

Ex. 2 to Targowska Decl. (Bates Nos. TQD000345 – TQD000356).

(4) Claim 19 of the U.S. Pat. No. 8,495,473:

[Preamble] An apparatus comprising:

[a] a multicarrier communications transceiver that is configured to

[a][1] perform an interleaving function associated with a first latency path and

[a][2] perform a deinterleaving function associated with a second latency path,

[b] the multicarrier communications transceiver being associated with a memory, wherein the memory is allocated between the interleaving function and the deinterleaving function in

> accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

Ex. 5 to Targowska Decl. (Bates Nos. TQD000486 – TQD000498).

CLAIM CONSTRUCTION FOR THE CLAIM TERMS OF THE FAMILY 3 PATENTS

Claim Term	Court's Construction
"shared memory"	"common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"
"amount of memory"	plain meaning
"the shared memory allocated to the [deinterleaver *I* interleaver] is used at the same time as the shared memory allocated to the [interleaver *I* deinterleaver]"	"the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"
"latency path"	"transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay"
"wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message"	plain meaning
"portion of memory"	plain meaning
"memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function"	"an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"
"wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function"	"wherein the generated message indicates the amount of memory that has been allocated to the [first deinterleaving / interleaving] function and the amount of memory allocated to the [second] deinterleaving function"

D.I. 454 (December 28, 2017).

Claim Term	Court's Construction
"transceiver"	"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"

D.I. 485 (February 6, 2018).

EXHIBIT 2

US008276048B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 8,276,048 B2**
(45) **Date of Patent: *Sep. 25, 2012**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

(75) Inventors: **Marcos C. Tzannes**, Orinda, CA (US); **Michael Lund**, West Newton, MA (US)

(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/901,699**

(22) Filed: **Oct. 11, 2010**

(65) **Prior Publication Data**

US 2011/0029844 A1 Feb. 3, 2011

Related U.S. Application Data

(63) Continuation of application No. 12/761,586, filed on Apr. 16, 2010, now Pat. No. 7,844,882, which is a continuation of application No. 11/246,163, filed on Oct. 11, 2005, now Pat. No. 7,831,890.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**

H03M 13/00	(2006.01)
H04B 1/38	(2006.01)
G06F 13/00	(2006.01)
G06F 15/16	(2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222; 711/147; 711/157; 709/215

(58) **Field of Classification Search** 714/774, 714/784; 375/222; 711/147, 157; 709/215
See application file for complete search history.

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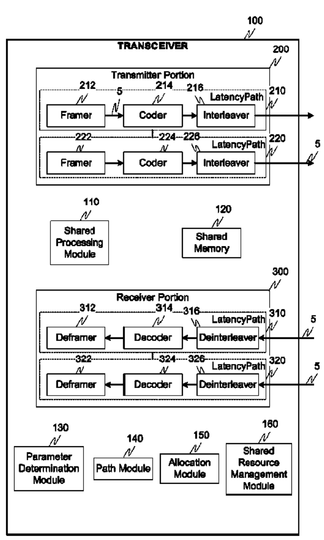
Primary Examiner — John J Tabone, Jr.
(74) *Attorney, Agent, or Firm* — Jason H. Vick; Sheridan Ross, PC

(57) **ABSTRACT**

A system allocates shared memory by transmitting/receiving a message specifying a maximum number of bytes of memory that are available to be allocated to an interleaver. The system determines an amount of memory required by the interleaver to interleave a first plurality of RS coded data bytes within a shared memory and allocates a first number of bytes of the shared memory to the interleaver to interleave the first plurality of RS coded data bytes for transmission at a first data rate. The system also allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate and interleaves the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaves the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

8 Claims, 3 Drawing Sheets



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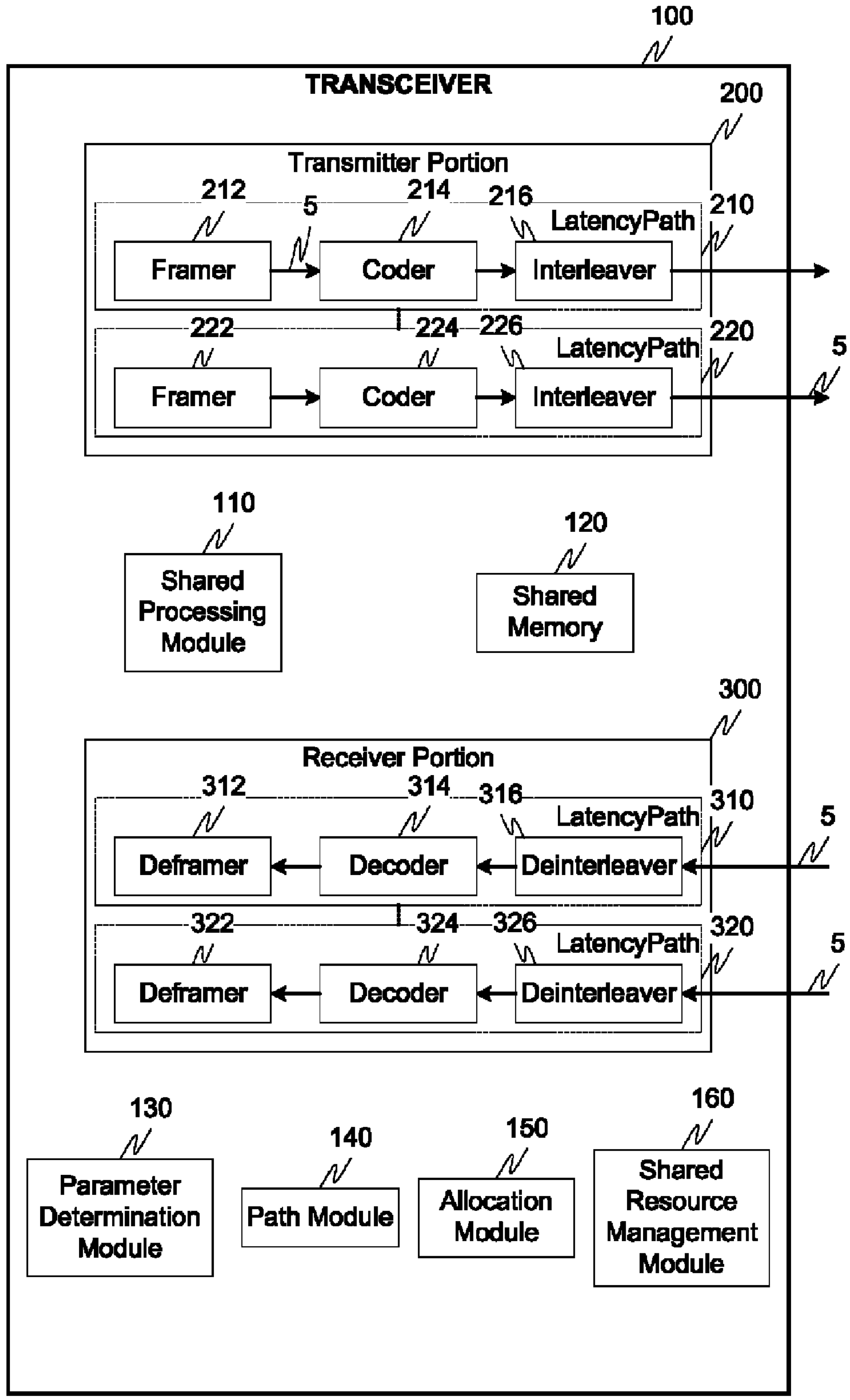
100
TRANSCEIVER
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Transmitter Portion
212
5
214
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LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

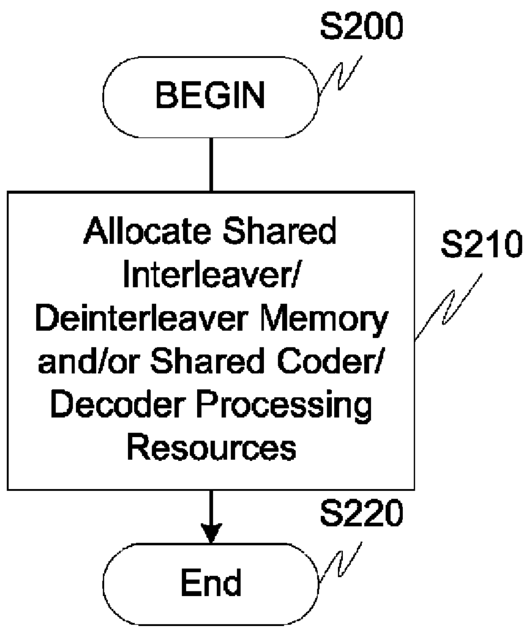
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

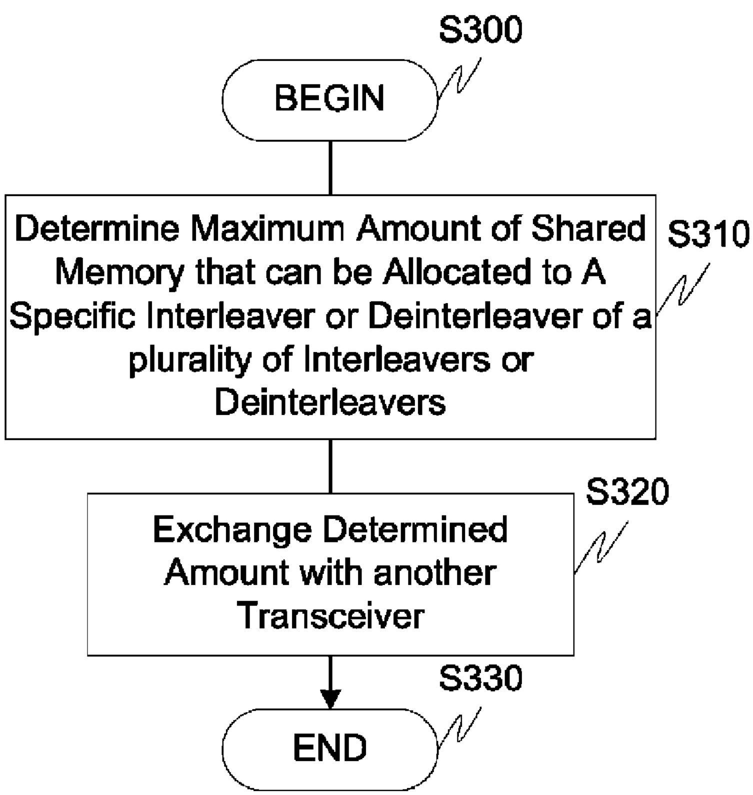
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

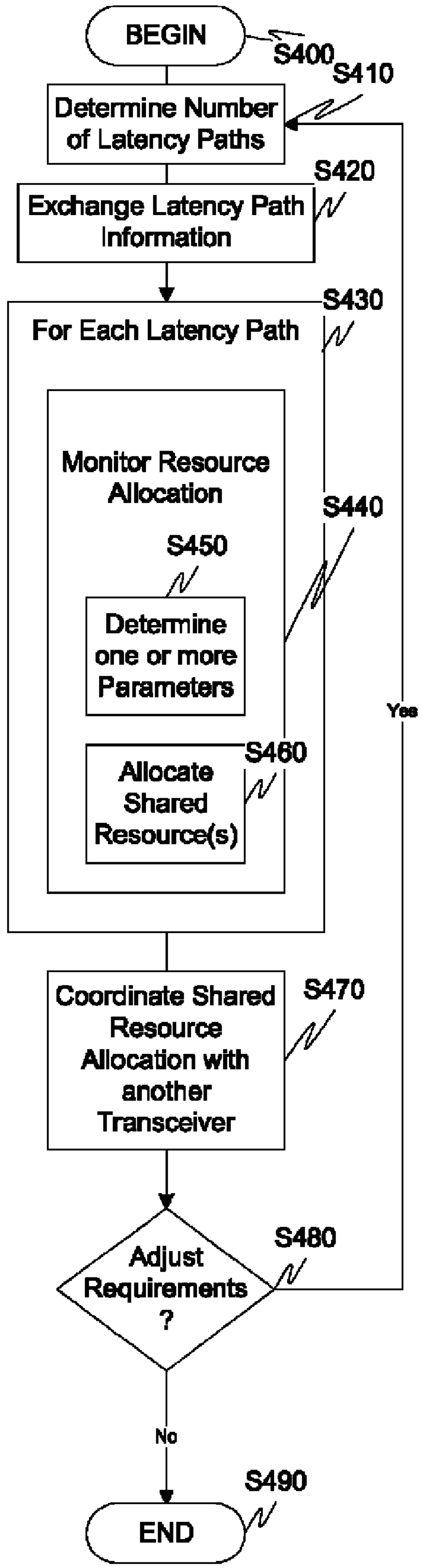
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
Yes
S460
Allocate Shared Resource(s)
Coordinate Shared Resource Allocation with another Transceiver
S470
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 12/761,586, filed Apr. 16, 2010, now U.S. Pat. No. 7,844,882, which is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, now U.S. Pat. No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention

relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel **5**, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver

100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such

as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

EXAMPLE #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

EXAMPLE #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

EXAMPLE #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g.,. N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is deter-

mined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined. Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The system of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The system of claim **1**, wherein the determining is based on a latency requirement.

4. The system of claim **1**, wherein the determining is based on a bit error rate requirement.

5. A system that allocates shared memory comprising:

a transceiver that is capable of:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The system of claim **5**, wherein the determining is based on an impulse noise protection requirement.

7. The system of claim **5**, wherein the determining is based on a latency requirement.

8. The system of claim **5**, wherein the determining is based on a bit error rate requirement.

* * * * *

EXHIBIT 3

US007844882B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 7,844,882 B2**
(45) **Date of Patent: *Nov. 30, 2010**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/761,586**

(22) Filed: **Apr. 16, 2010**

(65) **Prior Publication Data**

US 2010/0228924 A1 Sep. 9, 2010

Related U.S. Application Data

(63) Continuation of application No. 11/246,163, filed on Oct. 11, 2005.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222

(58) **Field of Classification Search** 709/215; 375/222; 714/774, 784; 711/147, 153, 157, 711/170, 173; 379/93.01
See application file for complete search history.

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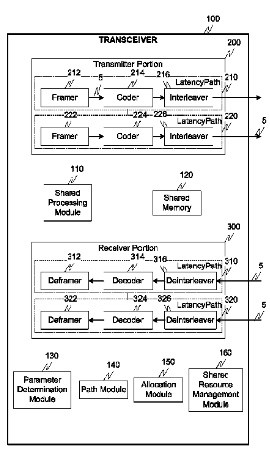
Primary Examiner—Joon H Hwang
Assistant Examiner—Mark Pfizenmayer
(74) *Attorney, Agent, or Firm*—Jason H. Vick; Sheridan Ross, P.C.

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

16 Claims, 3 Drawing Sheets



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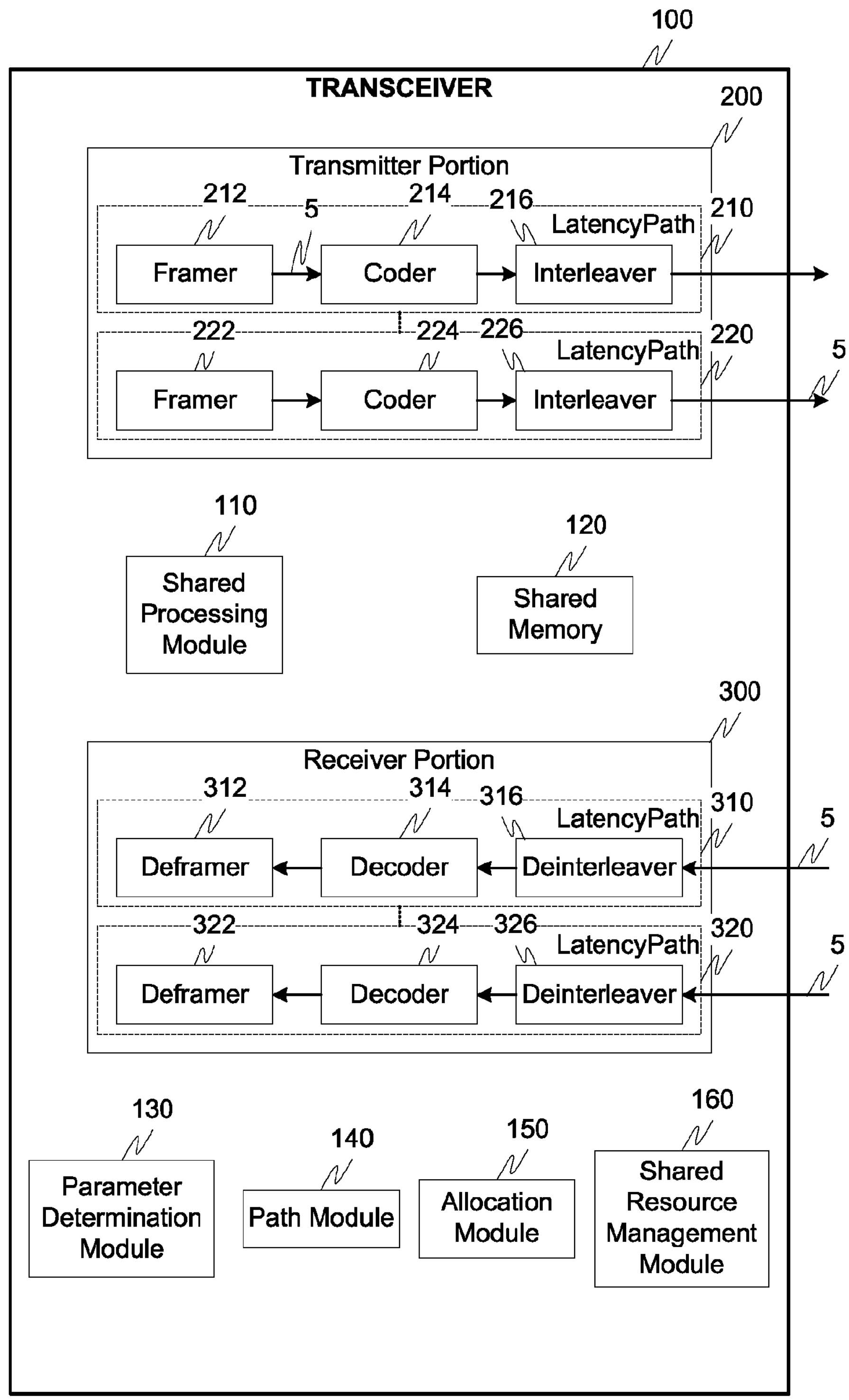
100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
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Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

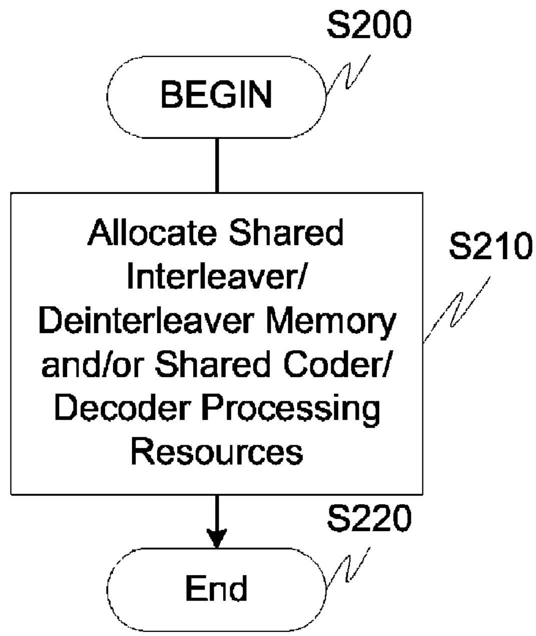
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

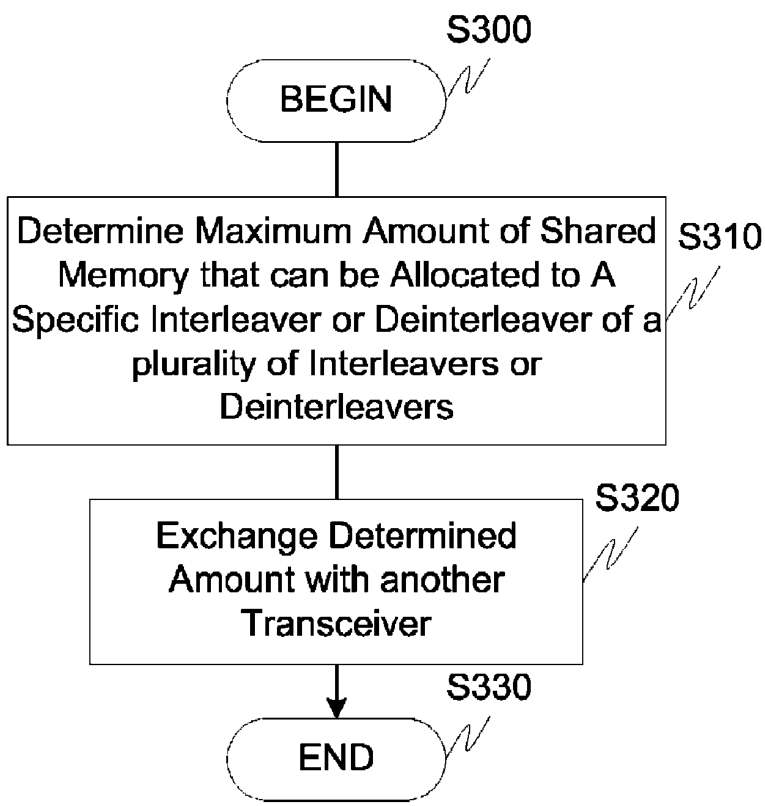
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

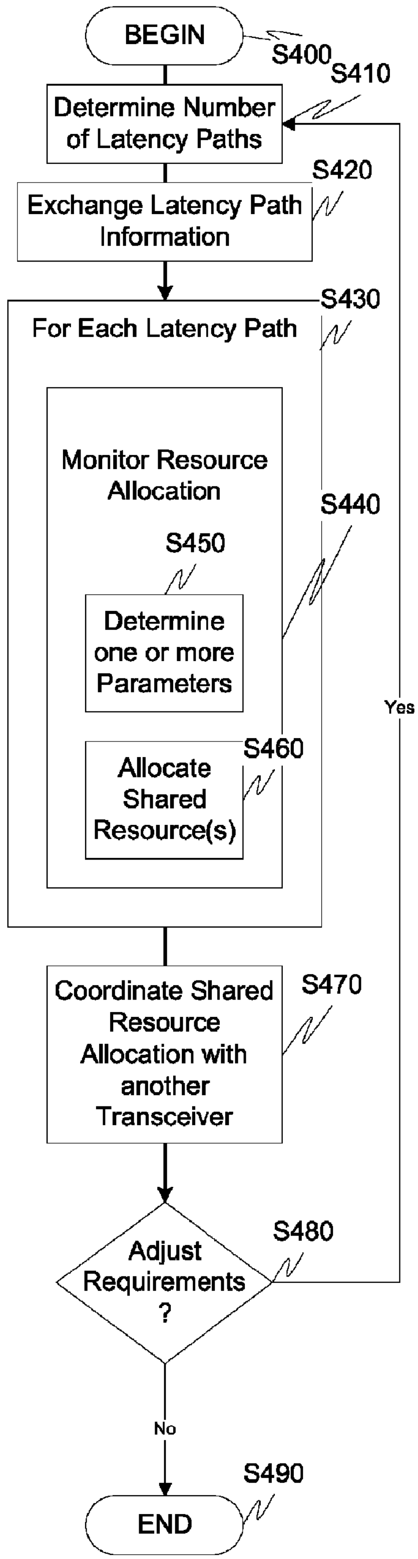
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
Coordinate Shared Resource Allocation with another Transceiver
S470
S480
Adjust Requirements ?
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel **5**, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of

transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or de-interleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in

ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support.

Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is determined. Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is

transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step **S330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step **S400** and continues to step **S410**. In step **S410**, the number of latency paths are determined Then, in step **S420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step **S430**.

In step **S430**, and for each latency path, the steps in step **440** are performed.

In step **S440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step **S450**, one or more parameters associated with the communication system are determined. Then, in step **S460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step **S470**.

In step **S470**, the allocation of shared resources is communicated to another transceiver. Next, in step **S480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step **S410**. Otherwise, control jumps to step **S490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation

platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A system for allocating shared memory comprising:

means for transmitting or receiving, by a transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

means for determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

means for allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

means for allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

means for interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The system of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The system of claim 1, wherein the determining is based on a latency requirement.

4. The system of claim 1, wherein the determining is based on a bit error rate requirement.

5. A system for allocating shared memory comprising:

means for transmitting or receiving, by a transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

means for determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

means for allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

means for allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

means for deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The system of claim 5, wherein the determining is based on an impulse noise protection requirement.

7. The system of claim 5, wherein the determining is based on a latency requirement.

8. The system of claim 5, wherein the determining is based on a bit error rate requirement.

9. A system that allocates shared memory comprising:

a transceiver that performs:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

10. The system of claim 9 wherein the determining is based on an impulse noise protection requirement.

11. The system of claim 9, wherein the determining is based on a latency requirement.

12. The system of claim 9, wherein the determining is based on a bit error rate requirement.

13. A system that allocates shared memory comprising:

a transceiver that performs:

transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

14. The system of claim 13, wherein the determining is based on an impulse noise protection requirement.

15. The system of claim 13, wherein the determining is based on a latency requirement.

16. The system of claim 13, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,844,882 B2
APPLICATION NO. : 12/761586
DATED : November 30, 2010
INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 11, claim 5, line 17, delete "transmission" and insert -- reception --

In column 11, claim 5, line 23, delete "received" and insert -- transmitted --

In column 11, claim 5, line 28, delete "shred" and insert -- shared --

In column 12, claim 13, line 29, delete "transmission" and insert -- reception --

In column 12, claim 13, line 35, delete "received" and insert -- transmitted --

In column 12, claim 13, line 40, delete "shred" and insert -- shared --

Signed and Sealed this
Third Day of May, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

EXHIBIT 4

US007836381B1

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.:** **US 7,836,381 B1**
(45) **Date of Patent:** ***Nov. 16, 2010**

(54) **COMPUTER READABLE MEDIUM WITH INSTRUCTIONS FOR RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

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(73) Assignee: **Aware, Inc.**, Bedford, MA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/853,020**

(22) Filed: **Aug. 9, 2010**

Related U.S. Application Data

(63) Continuation of application No. 11/246,163, filed on Oct. 11, 2005.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** **714/774**; 714/784; 375/222

(58) **Field of Classification Search** 709/215; 375/222; 714/774, 784; 711/147, 153, 157, 711/170, 173; 379/93.01
See application file for complete search history.

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(Continued)

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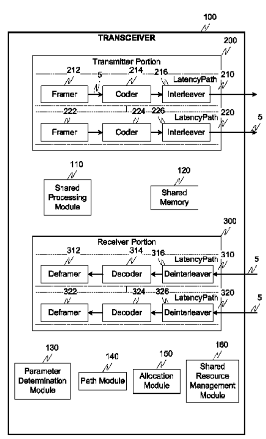
Assistant Examiner—Mark Pfizenmayer
(74) *Attorney, Agent, or Firm*—Jason H. Vick; Sheridan Ross P.C.

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

8 Claims, 3 Drawing Sheets



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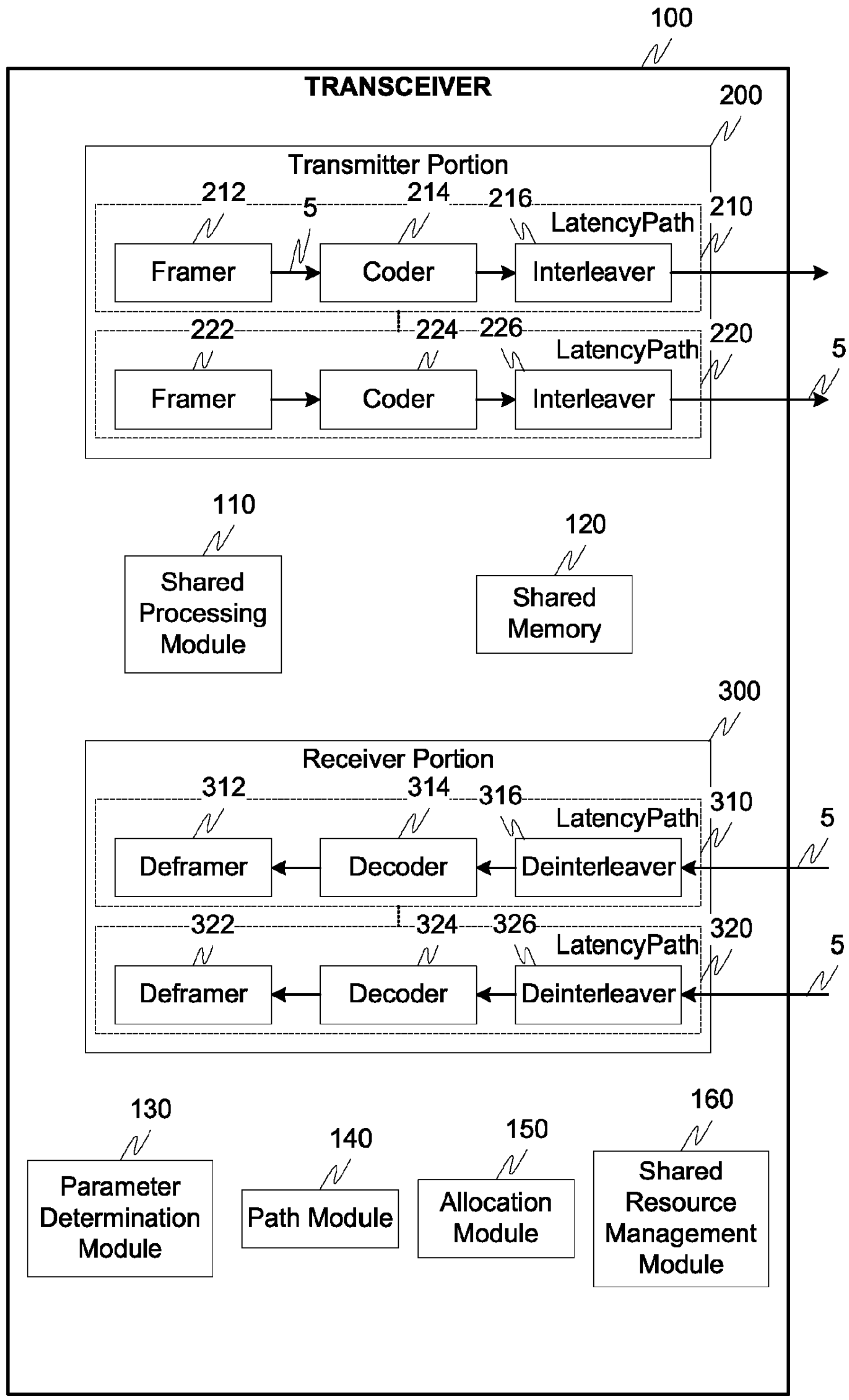
100
TRANSCEIVER
200
Transmitter Portion
212
5
214
216
LatencyPath
210
Framer
Coder
Interleaver
222
224
226
LatencyPath
220
5
Framer
Coder
Interleaver
110
Shared Processing Module
120
Shared Memory
300
Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
Deinterleaver
130
Parameter Determination Module
140
Path Module
150
Allocation Module
160
Shared Resource Management Module

Fig. 1

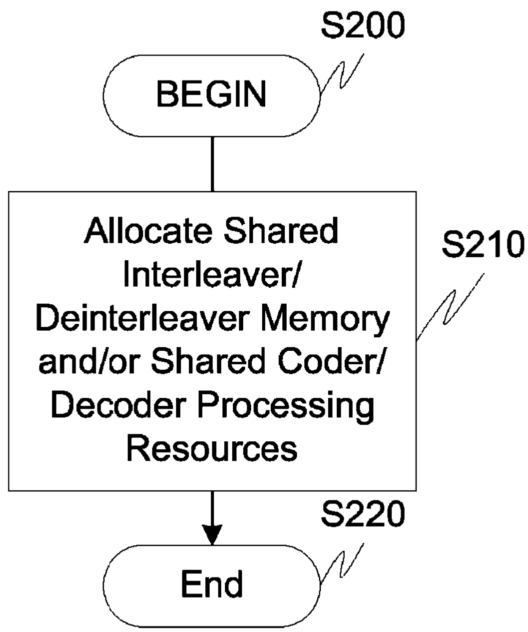
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

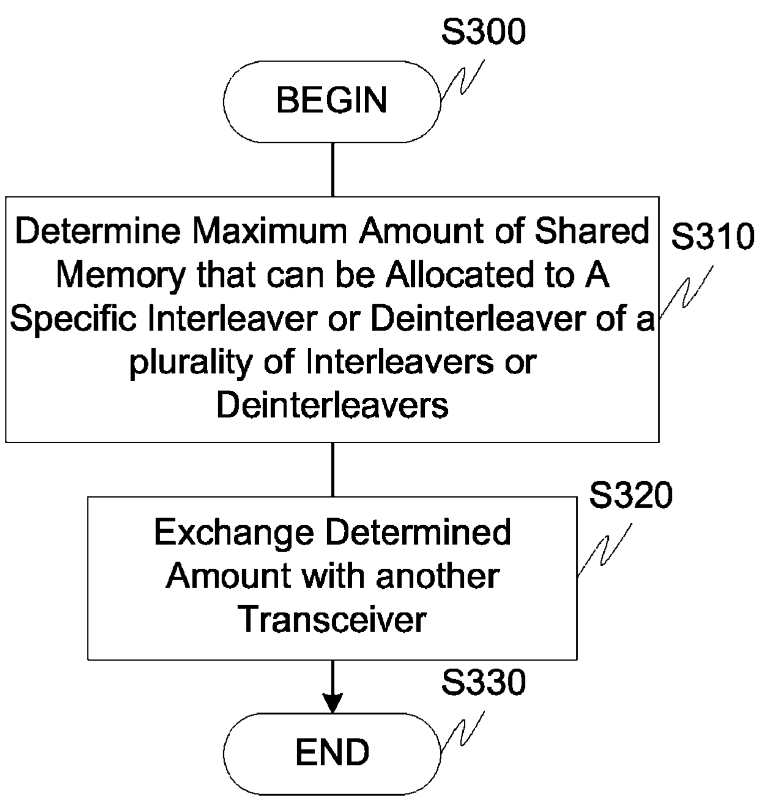
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

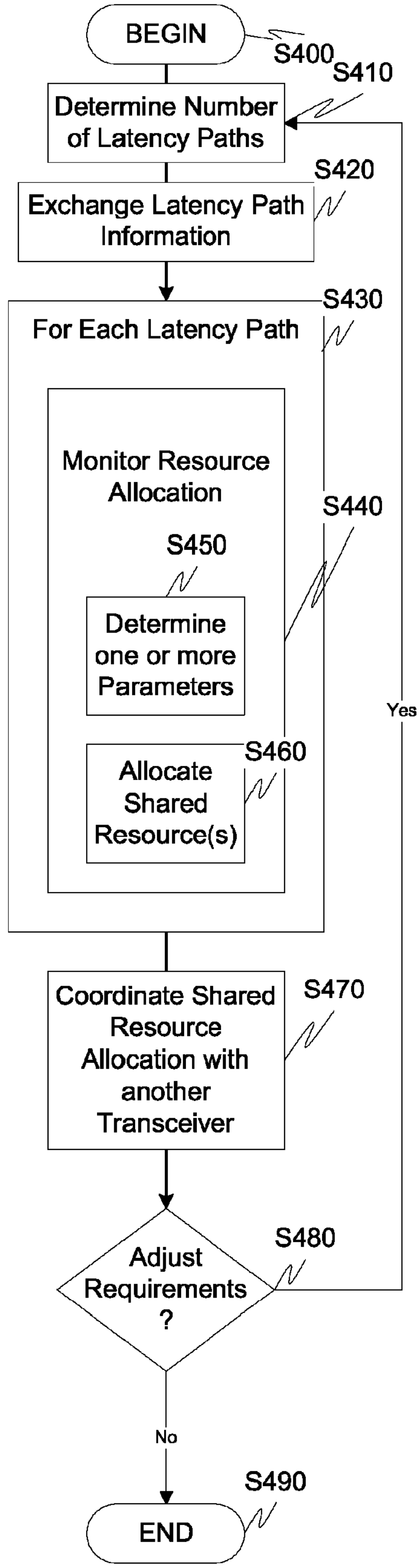
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
Yes
S460
Allocate Shared Resource(s)
Coordinate Shared Resource Allocation with another Transceiver
S470
S480
Adjust Requirements ?
No
S490
END

Fig. 4

COMPUTER READABLE MEDIUM WITH INSTRUCTIONS FOR RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,589 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system. More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof. Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver **100** can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of

transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined. The parameter determination module **130** then analyses one or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in

ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support.

Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3

Max Interleaver Memory for latency path #1=16 Kbytes

Max Interleaver Memory for latency path #2=16 Kbytes

Max Interleaver Memory for latency path #3=16 Kbytes

Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64

latency path #2—Video: N=128, R=8, D=32

latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50

latency path #2—Video: N=200, R=10, D=50

latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plural-

ity of interleavers or deinterleavers in a transceiver is determined. Next, in step **S320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step **S330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step **S400** and continues to step **S410**. In step **S410**, the number of latency paths are determined. Then, in step **S420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step **S430**.

In step **S430**, and for each latency path, the steps in step **440** are performed.

In step **S440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step **S450**, one or more parameters associated with the communication system are determined. Then, in step **S460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step **S470**.

In step **S470**, the allocation of shared resources is communicated to another transceiver. Next, in step **S480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step **S410**. Otherwise, control jumps to step **S490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;

determining, at the transceiver, an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and

interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data

bytes within the shared memory allocated to the deinterleaver, wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

2. The media of claim **1**, wherein the determining is based on an impulse noise protection requirement.

3. The media of claim **1**, wherein the determining is based on a latency requirement.

4. The media of claim **1**, wherein the determining is based on a bit error rate requirement.

5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:

transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;

allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;

allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate; and

deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shred memory allocated to the interleaver, wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

6. The media of claim **5**, wherein the determining is based on an impulse noise protection requirement.

7. The media of claim **5**, wherein the determining is based on a latency requirement.

8. The media of claim **5**, wherein the determining is based on a bit error rate requirement.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,836,381 B1
APPLICATION NO. : 12/853020
DATED : November 16, 2010
INVENTOR(S) : Marcos C. Tzannes et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 12, claim 5, line 2, delete "transmission" and insert -- reception --

In column 12, claim 5, line 7, delete "received" and insert -- transmitted --

In column 12, claim 5, line 12, delete "shred" and insert -- shared --

Signed and Sealed this
Eighth Day of February, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office

EXHIBIT 5

US008495473B2

(12) **United States Patent**
Tzannes et al.

(10) **Patent No.: US 8,495,473 B2**
(45) **Date of Patent: Jul. 23, 2013**

(54) **RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT**

(75) Inventors: **Marcos C. Tzannes**, Orinda, CA (US); **Michael Lund**, West Newton, MA (US)

(73) Assignee: **TQ Delta, LLC**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/567,261**

(22) Filed: **Aug. 6, 2012**

(65) **Prior Publication Data**

US 2012/0297148 A1 Nov. 22, 2012

Related U.S. Application Data

(63) Continuation of application No. 12/901,699, filed on Oct. 11, 2010, now Pat. No. 8,276,048, which is a continuation of application No. 12/761,586, filed on Apr. 16, 2010, now Pat. No. 7,844,882, which is a continuation of application No. 11/246,163, filed on Oct. 11, 2005, now Pat. No. 7,831,890.

(60) Provisional application No. 60/618,269, filed on Oct. 12, 2004.

(51) **Int. Cl.**

H03M 13/00	(2006.01)
H04B 1/38	(2006.01)
G06F 13/00	(2006.01)
G06F 15/16	(2006.01)

(52) **U.S. Cl.**
USPC **714/774**; 714/784; 375/222; 711/147; 711/157; 709/215

(58) **Field of Classification Search**
USPC 714/774, 784; 375/222; 711/147, 711/157; 709/215
See application file for complete search history.

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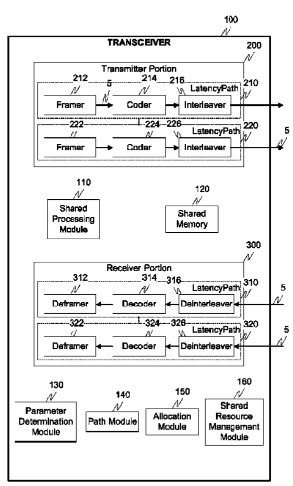
Primary Examiner — John J Tabone, Jr.
(74) *Attorney, Agent, or Firm* — Jason H. Vick; Sheridan Ross, PC

(57) **ABSTRACT**

A transceiver is designed to share memory and processing power amongst a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

46 Claims, 3 Drawing Sheets



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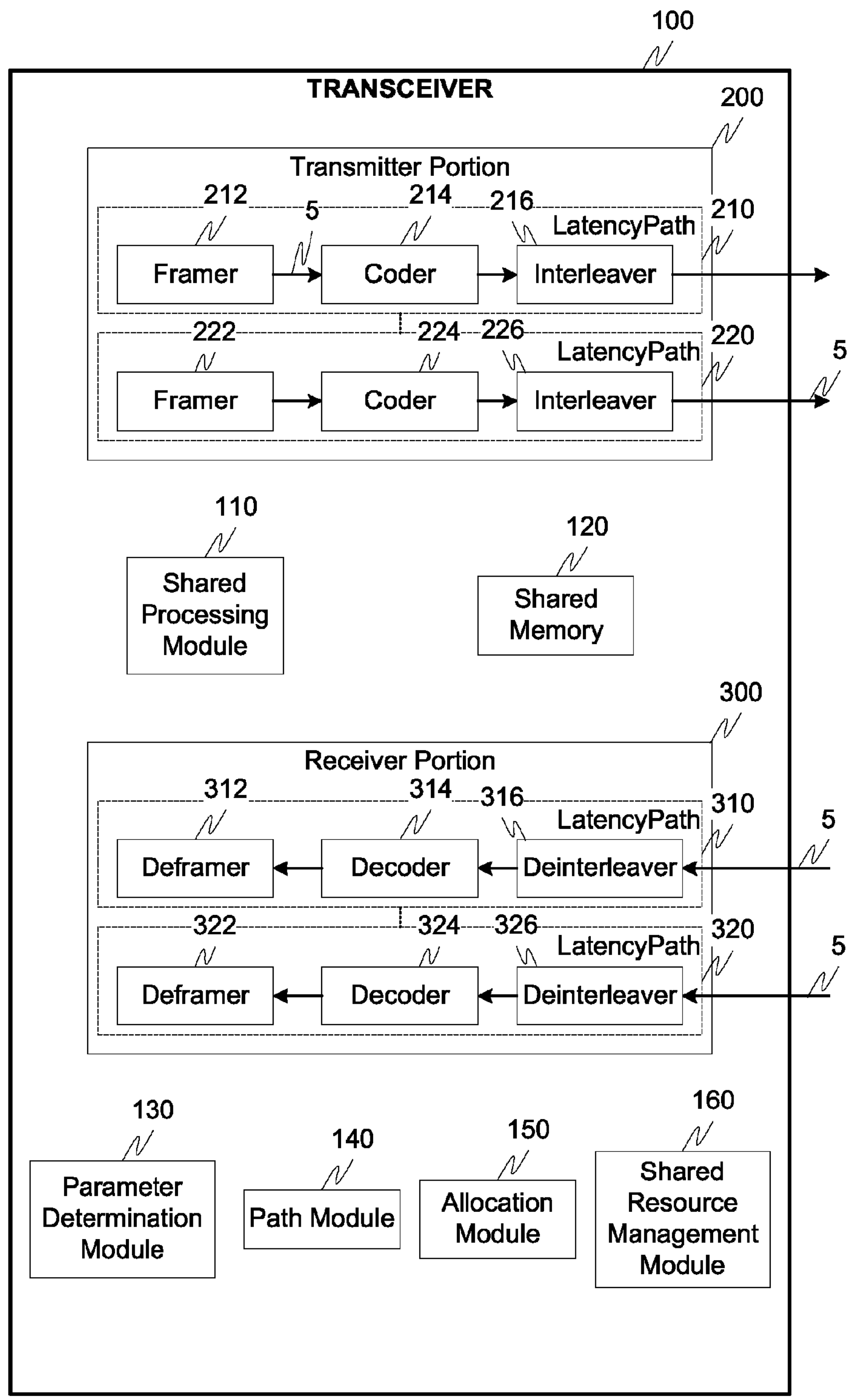
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Framer
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Interleaver
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224
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220
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Framer
Coder
Interleaver
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Shared
Processing
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Receiver Portion
312
314
316
LatencyPath
310
5
Deframer
Decoder
Deinterleaver
322
324
326
LatencyPath
320
5
Deframer
Decoder
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Allocation
Module
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Shared
Resource
Management
Module

Fig. 1

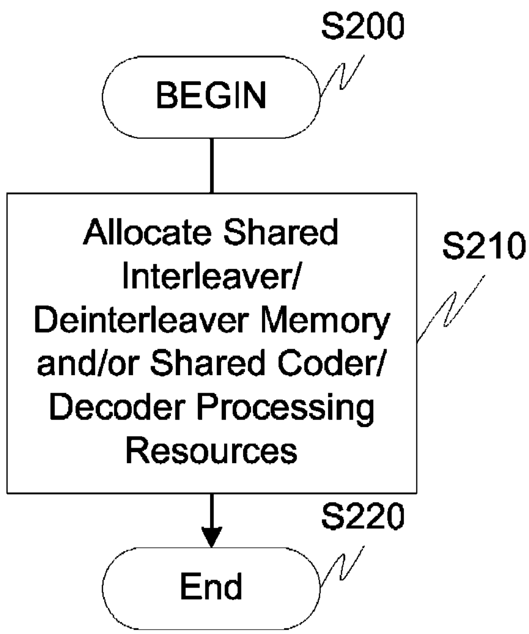
S200
BEGIN
Allocate Shared Interleaver/ Deinterleaver Memory and/or Shared Coder/ Decoder Processing Resources
S210
S220
End

Fig. 2

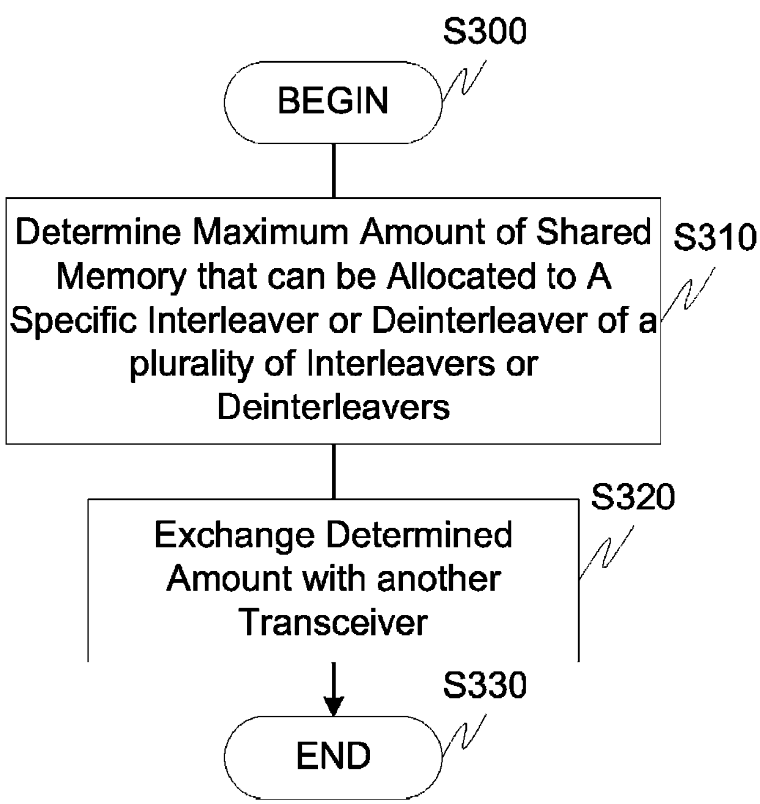
S300
BEGIN
Determine Maximum Amount of Shared Memory that can be Allocated to A Specific Interleaver or Deinterleaver of a plurality of Interleavers or Deinterleavers
S310
Exchange Determined Amount with another Transceiver
S320
S330
END

Fig. 3

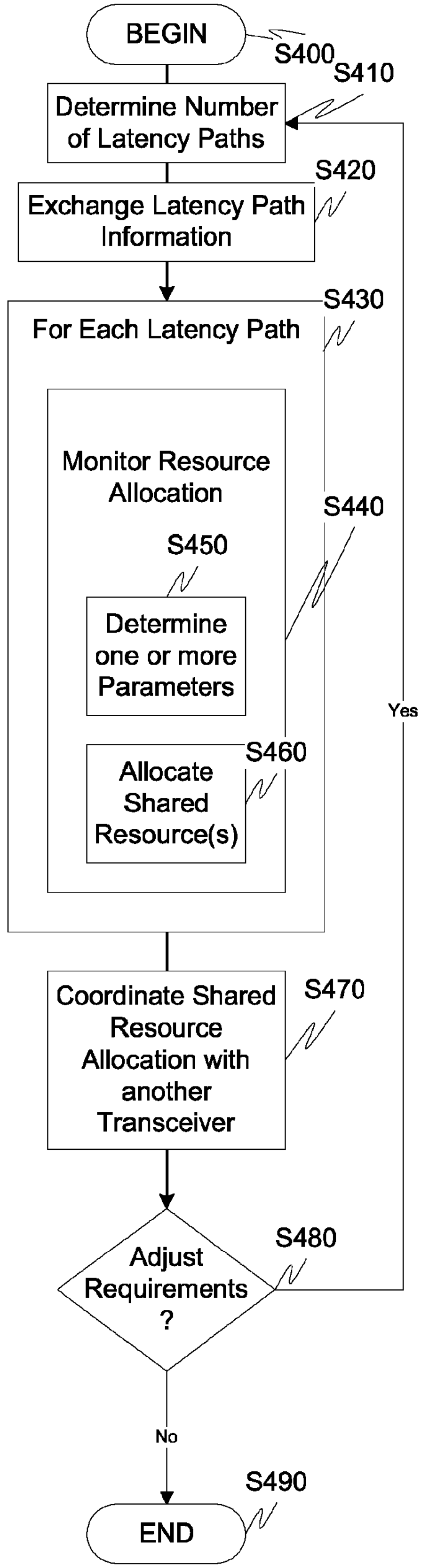
BEGIN
S400
S410
Determine Number of Latency Paths
S420
Exchange Latency Path Information
S430
For Each Latency Path
Monitor Resource Allocation
S440
S450
Determine one or more Parameters
S460
Allocate Shared Resource(s)
Yes
Coordinate Shared Resource Allocation with another Transceiver
S470
Adjust Requirements ?
S480
No
S490
END

Fig. 4

RESOURCE SHARING IN A TELECOMMUNICATIONS ENVIRONMENT

RELATED APPLICATION DATA

This application is a Continuation of U.S. application Ser. No. 12/901,699, filed Oct. 11, 2010, now U.S. Pat. No. 8,276,048, which is a Continuation of Ser. No. 12/761,586, filed Apr. 16, 2010, now U.S. Pat. No. 7,844,882, which is a Continuation of U.S. application Ser. No. 11/246,163 filed Oct. 11, 2005, now U.S. Pat. No. 7,831,890, which claims the benefit of and priority under 35 U.S.C. §119(e) to U.S. Patent Application No. 60/618,269, filed Oct. 12, 2004, entitled "Sharing Memory and Processing Resources in DSL Systems," each of which are incorporated herein by reference in their entirety.

BACKGROUND

1. Field of the Invention

This invention generally relates to communication systems. More specifically, an exemplary embodiment of this invention relates to memory sharing in communication systems. Another exemplary embodiment relates to processing or coding resource sharing in a communication system.

2. Description of Related Art

U.S. Pat. Nos. 6,775,320 and 6,778,596 describe DSL systems supporting multiple applications and multiple framer/coder/interleaver FCI blocks (an FCI block is also referred to as a latency path). DSL systems carry applications that have different transmission requirements with regard to, for example, data rate, latency (delay), bit error rate (BER), and the like. For example, video typically requires a low BER (<1E-10) but can tolerate higher latency (>20 ms). Voice, on the other hand, typically requires a low latency (<1 ms) but can tolerate BER (>1E-3).

As described in U.S. Pat. No. 6,775,320, different applications can use different latency paths in order to satisfy the different application requirements of the communication system. As a result a transceiver must support multiple latency paths in order to support applications such as video, Internet access and voice telephony. When implemented in a transceiver, each of the latency paths will have a framer, coder, and interleaver block with different capabilities that depend on the application requirements.

SUMMARY

One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability. For example, a typical DSL transceiver will have at least one latency path with approximately 16 kbytes of memory for the interleaver. Likewise, the coding block, for example, a Reed Solomon coder, consumes a large amount of processing power. In general, as the number of latency paths increase, the memory and processing power requirements for a communication system become larger.

Accordingly, an exemplary aspect of this invention relates to sharing memory between one or more interleavers and/or deinterleavers in a transceiver. More particularly, an exemplary aspect of this invention relates to shared latency path memory in a transceiver.

Additional aspects of this invention relate to configuring and initializing shared memory in a communication system.

More particularly, an exemplary aspect of this invention relates to configuring and initializing interleaver/deinterleaver memory in a communication system.

Additional aspects of the invention relate to determining the amount of memory that can be allocated to a particular component by a communication system. More specifically, an exemplary aspect of the invention relates to determining the maximum amount of shared memory that can be allocated to one or more interleaves or deinterleavers.

According to another exemplary aspect of the invention, processing power is shared between a number of transceiver modules. More specifically, and in accordance with an exemplary embodiment of the invention, a coding module is shared between one or more coders and/or decoders.

Another exemplary embodiment of the invention relates to transitioning from a fixed memory configuration to a shared memory configuration during one or more of initialization and SHOWTIME (user data transmission).

An additional exemplary aspect of the invention relates to dynamically updating one or more of shared memory and processing resources based on changing communication conditions.

An additional exemplary aspect of the invention relates to updating one or more of shared memory and processing resources based on an updated communication parameter.

An additional exemplary aspect of the invention relates to updating the allocation of one or more of shared memory and processing resources based on an updated communication parameter(s).

Additional aspects of the invention relate to exchanging shared resource allocations between transceivers.

Additional exemplary aspects relate to a method of allocating shared memory in a transceiver comprising allocating the shared memory to a plurality of modules, wherein each of the plurality of modules comprise at least one interleaver, at least one deinterleaver or a combination thereof.

Still further aspects relate to the above method wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above method wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

Additional exemplary aspects relate to a transceiver comprising a plurality of modules each including at least one interleaver, at least one deinterleaver or a combination thereof and a shared memory designed to be allocated to a plurality of the modules.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise interleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise deinterleavers.

Still further aspects relate to the above transceiver wherein the plurality of modules comprise at least one interleaver and at least one deinterleaver.

These and other features and advantages of this invention are described in, or are apparent from, the following description of the embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be described in detail, with reference to the following figures, wherein:

FIG. **1** is a functional block diagram illustrating an exemplary transceiver according to this invention;

FIG. **2** is a flowchart outlining an exemplary method of sharing resources according to this invention;

FIG. **3** is a flowchart outlining an exemplary method of determining a maximum amount of shared memory according to this invention; and

FIG. **4** is a flowchart outlining an exemplary resource sharing methodology according to this invention.

DETAILED DESCRIPTION

The exemplary embodiments of this invention will be described in relation to sharing resources in a wired and/or wireless communications environment. However, it should be appreciated, that in general, the systems and methods of this invention will work equally well for any type of communication system in any environment.

The exemplary systems and methods of this invention will also be described in relation to multicarrier modems, such as DSL modems and VDSL modems, and associated communication hardware, software and communication channels. However, to avoid unnecessarily obscuring the present invention, the following description omits well-known structures and devices that may be shown in block diagram form or otherwise summarized.

For purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. It should be appreciated however that the present invention may be practiced in a variety of ways beyond the specific details set forth herein.

Furthermore, while the exemplary embodiments illustrated herein show the various components of the system collocated, it is to be appreciated that the various components of the system can be located at distant portions of a distributed network, such as a telecommunications network and/or the Internet, or within a dedicated secure, unsecured and/or encrypted system. Thus, it should be appreciated that the components of the system can be combined into one or more devices, such as a modem, or collocated on a particular node of a distributed network, such as a telecommunications network. As will be appreciated from the following description, and for reasons of computational efficiency, the components of the system can be arranged at any location within a distributed network without affecting the operation of the system. For example, the various components can be located in a Central Office modem (CO, ATU-C, VTU-O), a Customer Premises modem (CPE, ATU-R, VTU-R), a DSL management device, or some combination thereof Similarly, one or more functional portions of the system could be distributed between a modem and an associated computing device.

Furthermore, it should be appreciated that the various links, including communications channel 5, connecting the elements can be wired or wireless links, or any combination thereof, or any other known or later developed element(s) that is capable of supplying and/or communicating data to and from the connected elements. The term module as used herein can refer to any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element. The terms determine, calculate and compute, and variations thereof, as used herein are used interchangeably and include any type of methodology, process, mathematical operation or technique. FCI block and latency path are used interchangeably herein as well as transmitting modem and transmitting transceiver. Receiving modem and receiving transceiver are also used interchangeably.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100** that utilizes shared resources. It should be appreciated that numerous functional components of the transceiver have been omitted for clarity. However, the transceiver

100 can also include the standard components found in typical communications device(s) in which the technology of the subject invention is implemented into.

According to an exemplary embodiment of the invention, memory and processing power can be shared among a plurality of transmitter and/or receiver latency paths, in a communications transceiver that carries or supports multiple applications. For example, the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path. This allocation can be done based on the data rate, latency, BER, impulse noise protection requirements of the application, data or information being transported over each latency path, or in general any parameter associated with the communications system.

Likewise, for example, the transmitter and/or receiver latency paths can share a Reed-Solomon coder/decoder processing module and the processing power of this module can be allocated to each encoder and/or decoder. This allocation can be done based on the data rate/latency, BER, impulse noise protection requirements of the application data or information being transported over each latency path, or in general based on any parameter associated with the communication system.

In accordance with an exemplary operational embodiment, a first transceiver and a second transceiver transmit to one another messages during, for example, initialization which contain information on the total and/or shared memory capabilities of each transceiver and optionally information about the one or more latency paths. This information can be transmitted prior to determining how to configure the latency paths to support the application requirements. Based on this information, one of the modems can select an FCI configuration parameter(s) that meets the transmission requirements of each application being transported over each latency paths. While an exemplary of the embodiment of the invention will be described in relation to the operation of the invention and characteristics thereof being established during initialization, it should be appreciated that the sharing of resources can be modified and messages transmitted between a two transceivers at any time during initialization and/or user data transmission, i.e., SHOWTIME.

FIG. **1** illustrates an exemplary embodiment of a transceiver **100**. The transceiver **100** includes a transmitter portion **200** and a receiver portion **300**. The transmitter portion **200** includes one or more latency paths **210**, **220**, ... Similarly, the receiver portion **300** includes one or more latency paths **310**, **320**, ... Each of the latency paths in the transmitter portion **200** includes a framer, coder, and interleaver designated as **212**, **214**, **216** and **222**, **224** and **226**, respectively. Each of the latency paths in the receiver portion includes a deframer, decoder, and deinterleaver designated as **312**, **314**, **316** and **322**, **324**, and **326**, respectively. The transceiver **100** further includes a shared processing module **110**, a shared memory **120**, a parameter determination module **130**, a path module **140**, an allocation module **150**, and a shared resource management module **160**, all interconnected by one or more links (not shown).

In this exemplary embodiment, the transceiver **100** is illustrated with four total transmitter portion and receiver portion latency paths, i.e., **210**, **220**, **310**, and **320**. The shared memory **120** is shared amongst the two transmitter portion interleavers **216** and **226** and two receiver portion deinterleavers **316** and **326**. The shared processing module **110**, such

as a shared coding module, is shared between the two transmitter portion coders **214** and **224** and the two receiver portion decoders **314** and **324**.

While the exemplary embodiment of the invention will be described in relation to a transceiver having a number of transmitter portion latency paths and receiver portion latency paths, it should be appreciated that this invention can be applied to any transceiver having any number of latency paths. Moreover, it should be appreciated that the sharing of resources can be allocated such that one or more of the transmitter portion latency paths are sharing a shared resource, one or more of the receiver portion latency paths are sharing a shared resource, or a portion of the transmitter portion latency paths and a portion of the receiver portion latency paths are sharing shared resources. Moreover, any one or more of the latency paths, or portions thereof, could also be assigned to a fixed resource while, for example, another portion of the latency path(s) assigned to a shared resource. For example, in latency path **210**, the interleaver **216** could be allocated a portion of the shared memory **120**, while the coder **214** could be allocated to a dedicated processing module, vice versa, or the like.

In accordance with the exemplary embodiment, a plurality of transmitter portion or receiver portion latency paths share an interleaver/deinterleaver memory, such as shared memory **120**, and a coding module, such as shared processing module **110**. For example, the interleaver/deinterleaver memory can be allocated to different interleavers and/or deinterleavers. This allocation can be based on parameters associated with the communication systems such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported. Similarly, a coding module, which can be a portion of the shared processing module **110**, can be shared between any one or more of the latency paths. This sharing can be based on requirements such as data rate, latency, BER, impulse noise protection, and the like, of the applications being transported.

For example, an exemplary transceiver could comprise a shared interleaver/deinterleaver memory and could be designed to allocate a first portion of the shared memory **120** to an interleaver, such as interleaver **216** in the transmitter portion of the transceiver and allocate a second portion of the shared memory **120** to a deinterleaver, such as **316**, in the receiver portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory, such as shared memory **120**, and be designed to allocate a first portion of shared memory **120** to a first interleaver, e.g., **216**, in the transmitter portion of the transceiver and allocate a second portion of the shared memory to a second interleaver, e.g., **226**, in the transmitter portion of the transceiver.

Alternatively, for example, an exemplary transceiver can comprise a shared interleaver/deinterleaver memory and be designed to allocate a first portion of the shared memory **120** to a first deinterleaver, e.g., **316**, in the receiver portion of the transceiver and allocate a second portion of the shared memory to a second deinterleaver, e.g., **326**, in the receiver portion of the transceiver. Regardless of the configuration, in general any interleaver or deinterleaver, or grouping thereof, be it in a transmitter portion or receiver portion of the transceiver, can be associated with a portion of the shared memory **120**.

Establishment, configuration and usage of shared resources is performed in the following exemplary manner. First, and in cooperation with the path module **140**, the number of transmitter and receiver latency paths (N) is determined The parameter determination module **130** then analyses one

or more parameters such as data rate, transmitter data rate, receiver data rate, impulse noise protection, bit error rate, latency, or the like. Based on one or more of these parameters, the allocation module **150** allocates a portion of the shared memory **120** to one or more of the interleaver and/or deinterleavers, or groupings thereof. This process continues until the memory allocation has been determined and assigned to each of the N latency paths.

Having determined the memory allocation for each of the latency paths, and in conjunction with the shared resource management **160**, the transceiver **100** transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths.

Three examples of sharing interleaver/deinterleaver memory and coding processing in a transceiver are described below. The latency paths in these examples can be in the transmitter portion of the transceiver or the receiver portion of the transceiver.

Example #1

A first transmitter portion or receiver portion latency path may carry data from a video application, which needs a very low BER but can tolerate higher latency. In this case, the video will be transported using an latency path that has a large amount of interleaving/deinterleaving and coding (also known as Forward Error Correction (FEC) coding). For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 255 bytes (N=255) with 16 checkbytes (R=16) and interleaving/deinterleaving using an interleaver depth of 64 (D=64). This latency path will require N*D=255*64=16 Kbytes of interleaver memory at the transmitter (or deinterleaver memory at the receiver). This latency path will be able to correct a burst of errors that is less than 512 bytes in duration.

A second transmitter portion or receiver portion latency path may carry an internet access application that requires a medium BER and a medium amount of latency. In this case, the internet access application will be transported using a latency path that has a medium amount of interleaving and coding. For example, the latency path may be configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 1 (D=32). This latency path will require N*D=128*32=4 Kbytes of interleaver memory and the same amount of deinterleaver memory. This latency path will be able to correct a burst of errors that is less than 128 bytes in duration.

A third transmitter portion or receiver portion latency path may carry a voice telephony application, which needs a very low latency but can tolerate BER. In this case, the video will be transported using an latency path that has a large amount of interleaving and coding. For example, the third transmitter portion or receiver portion latency path may be configured with no interleaving or coding which will result in the lowest possible latency through the latency path but will provide no error correction capability.

According to the principles of this invention, a system carrying the three applications described above in Example #1, would have three latency paths that share one memory space containing at least (16+4)=20 Kbytes. The three latency paths also share a common coding block that is able to simultaneously encode (in the transmitter portion) or decode (in a receiver portion) two codewords with N=255/R=16 and N=128/R=8.

According to an exemplary embodiment of this invention, the latency paths can be reconfigured at initialization or during data transmission mode (also known as SHOWTIME in ADSL and VDSL transceivers). This would occur if, for example, the applications or application requirements were to change.

Example #2

If instead of 1 video application, 1 internet application and 1 voice application, there were 3 internet access applications then the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory and coding module in a different way. For example, the system could be reconfigured to have 3 transmitter portion or receiver portion latency paths, with each latency path being configured with Reed-Solomon coding using a codeword size of 128 bytes (N=128) with 8 checkbytes (R=8) and interleaving using an interleaver depth of 16 (D=32). Each latency path will require N*D=128*32=4 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 128 bytes in duration. Based on the example of carrying the three internet access applications described, the three latency path share one memory space containing at least 3*4=12 Kbytes. Also the three latency paths share a common coding block that is able to simultaneously encode (on the transmitter side) or decode (on the receiver side) three codewords with N=128/R=16, N=128/R=8 and N=128/R=8.

Example #3

The system could be configured to carry yet another set of applications. For example, the latency paths could be configured to carry 2 video applications. In this case only 2 transmitter portion or receiver portion latency paths are needed, which means that the third latency path could be simply disabled. Also, assuming that the memory is constrained based on the first example above, then the maximum shared memory for these 2 latency paths is 20 kBytes. In this case, the system could be reconfigured to have 2 latency paths, with each block being configured with Reed-Solomon coding using a codeword size of 200 bytes (N=200) with 10 checkbytes (R=10) and interleaving/deinterleaving using an interleaver depth of 50 (D=50). Each latency path will require N*D=200*50=10 Kbytes of interleaver memory and each block will be able to correct a burst of errors that is less than 250 bytes in duration. This configuration results in 20K of shared memory for both latency paths, which is the same as in the first example. In order to stay within the memory constraints of the latency paths, the error correction capability for each latency path is decreased to 250 bytes from 512 bytes in Example #1.

Another aspect of this invention is the how FCI configuration information is transmitted between a first modem and a second modem. FCI configuration information will depend on the requirements of the applications being transported over the DSL connection. This information may need to be forwarded during initialization in order to initially configure the DSL connection. This information may also need to be forwarded during SHOWTIME in order to reconfigure the DSL connection based on a change in applications or the application requirements.

According to one embodiment, a first modem determines the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. In order to determine the FCI configuration parameters, the first modem must know what are the capabilities of a second modem. For example, the first modem must know how many latency paths (FCI blocks) the second modem can support. Also the first modem must know the maximum amount of interleaver memory for each transmitter latency path. In addition, since the transmitter latency paths may share a common memory space the first modem must know the total shared memory for all transmitter latency paths. This way the first modem will be able to choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem.

For example, using values from examples above, a first transceiver could send a message to a second transceiver during initialization or during SHOWTIME containing the following information:

Number of supported transmitter and receiver latency paths=3
Max Interleaver Memory for latency path #1=16 Kbytes
Max Interleaver Memory for latency path #2=16 Kbytes
Max Interleaver Memory for latency path #3=16 Kbytes
Maximum total/shared memory for all latency paths=20 kBytes

Based on this information, and the application requirements, the first transceiver would select latency path settings. For example, if the applications are 1 video, 1 internet access and 1 voice application, the first transceiver could configure 3 latency paths as follows:

latency path #1—Video: N=255, R=16, D=64
latency path #2—Video: N=128, R=8, D=32
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would result in a total interleaver memory of 20 kbytes.

Alternatively, if for example, there are only 2 video applications, the first transceiver could configure 2 latency paths as follows:

latency path #1—Video: N=200, R=10, D=50
latency path #2—Video: N=200, R=10, D=50
latency path #3—Video: N=0, R=0, D=1 (no coding or interleaving)

This would also result in a total interleaver memory of 20 kbytes.

Alternatively, the second transceiver can determine the specific FCI configuration parameters, e.g., N, D, R as defined above, needed to meet specific application requirements, such as latency, burst error correction capability, etc. As described above for the first transceiver, in order to determine the FCI configuration parameters, the second transceiver must first know what are the capabilities of the first transceiver. In this case, the first transceiver would send a message to the second transceiver containing the information described above and based on this information and the application requirements the second transceiver would select latency path settings.

FIG. **2** outlines an exemplary method of allocating shared memory in a transceiver. More specifically, control begins in step S**200** and continues to step S**210**. In step S**210**, one or more of shared interleaver/deinterleaver memory and/or shared coder/decoder processing resources are allocated to one or more latency paths, in a transceiver. Control then continues to step S**220** where the control sequence ends.

FIG. **3** outlines an exemplary method of exchanging shared resource allocations according to an exemplary embodiment of this invention. In particular, control begins in step S**310**. In step S**310**, a maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers or deinterleavers in a transceiver is deter-

mined Next, in step S**320**, the determined maximum amount for one or more of the deinterleavers and/or interleavers is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. Control then continues to step S**330** where the control sequence ends.

FIG. **4** outlines an exemplary procedure for resource sharing according to an exemplary embodiment of this invention. In particular, control begins in step S**400** and continues to step S**410**. In step S**410**, the number of latency paths are determined Then, in step S**420**, the latency path information (FCI block information) is transmitted to another transceiver. Messages containing additional information can also be transmitted to the other transceiver and/or received from the other transceiver. This information can be used to, for example, assist with the determination of memory allocation in the transceiver. Moreover, the messages received from the other transceiver could specify what the memory allocation is to be based on, for example, the number of latency paths, memory allocation in the remote transceiver and required applications. Control then continues to step S**430**.

In step S**430**, and for each latency path, the steps in step **440** are performed.

In step S**440**, and while monitoring of allocation of resources is being performed, steps **450** and **460** are performed. More specifically, in step S**450**, one or more parameters associated with the communication system are determined Then, in step S**460**, shared resources are allocated based on one or more of the communication parameters. Control then continues to step S**470**.

In step S**470**, the allocation of shared resources is communicated to another transceiver. Next, in step S**480**, a determination is made as to whether there is a change in communications that would require the adjustment of the shared resource allocation. Examples of changes in communications conditions include a change in applications being transported over the system and/or changes in the channel condition, etc. If adjustments are required, control jumps back to step S**410**. Otherwise, control jumps to step S**490** where the control sequence ends.

The above-described system can be implemented on wired and/or wireless telecommunications devices, such a modem, a multicarrier modem, a DSL modem, an ADSL modem, an XDSL modem, a VDSL modem, a linecard, test equipment, a multicarrier transceiver, a wired and/or wireless wide/local area network system, a satellite communication system, a modem equipped with diagnostic capabilities, or the like, or on a separate programmed general purpose computer having a communications device or in conjunction with any of the following communications protocols: CDSL, ADSL2, ADSL2+, VDSL1, VDSL2, HDSL, DSL Lite, IDSL, RADSL, SDSL, UDSL or the like.

Additionally, the systems, methods and protocols of this invention can be implemented on a special purpose computer, a programmed microprocessor or microcontroller and peripheral integrated circuit element(s), an ASIC or other integrated circuit, a digital signal processor, a hard-wired electronic or logic circuit such as discrete element circuit, a programmable logic device such as PLD, PLA, FPGA, PAL, a modem, a transmitter/receiver, any comparable means, or the like. In general, any device capable of implementing a state machine that is in turn capable of implementing the methodology illustrated herein can be used to implement the various communication methods, protocols and techniques according to this invention.

Furthermore, the disclosed methods may be readily implemented in software using object or object-oriented software development environments that provide portable source code that can be used on a variety of computer or workstation platforms. Alternatively, the disclosed system may be implemented partially or fully in hardware using standard logic circuits or VLSI design. Whether software or hardware is used to implement the systems in accordance with this invention is dependent on the speed and/or efficiency requirements of the system, the particular function, and the particular software or hardware systems or microprocessor or microcomputer systems being utilized. The communication systems, methods and protocols illustrated herein can be readily implemented in hardware and/or software using any known or later developed systems or structures, devices and/or software by those of ordinary skill in the applicable art from the functional description provided herein and with a general basic knowledge of the computer and telecommunications arts.

Moreover, the disclosed methods may be readily implemented in software that can be stored on a storage medium, executed on programmed general-purpose computer with the cooperation of a controller and memory, a special purpose computer, a microprocessor, or the like. In these instances, the systems and methods of this invention can be implemented as program embedded on personal computer such as an applet, JAVA® or CGI script, as a resource residing on a server or computer workstation, as a routine embedded in a dedicated communication system or system component, or the like. The system can also be implemented by physically incorporating the system and/or method into a software and/or hardware system, such as the hardware and software systems of a communications transceiver.

It is therefore apparent that there has been provided, in accordance with the present invention, systems and methods for sharing resources. While this invention has been described in conjunction with a number of embodiments, it is evident that many alternatives, modifications and variations would be or are apparent to those of ordinary skill in the applicable arts. Accordingly, it is intended to embrace all such alternatives, modifications, equivalents and variations that are within the spirit and scope of this invention.

The invention claimed is:

1. A method for sharing resources in a multicarrier transceiver comprising:

sharing, in the transceiver, memory between an interleaver in a first latency path and a deinterleaver in a second latency path; and

transmitting or receiving, during initialization of the transceiver, a message, the message indicating how the shared memory is to be allocated to the interleaver in the first latency path or how the shared memory is to be allocated to the deinterleaver in the second latency path.

2. The method of claim **1**, wherein the transceiver is connected to a second transceiver using a wired or wireless channel and the transceivers are used to transport video, internet access and voice data.

3. The method of claim **1**, wherein the method is performed in a linecard that is capable of transporting video.

4. The method of claim **1**, wherein the method is performed in a customer premises modem that is capable of transporting video.

5. The method of claim **1**, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules.

6. The method of claim **1**, wherein the allocating of at least one portion of the shared memory is based on one or more communication parameters.

7. The method of claim **6**, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

8. The method of claim **1**, wherein the transceiver includes at least one digital signal processor.

9. The method of claim **1**, wherein the transceiver includes at least one ASIC.

10. A multicarrier communications transceiver with a shared memory, the transceiver capable of:

sharing the memory between an interleaver in a first latency path and

a deinterleaver in a second latency path; and

transmitting or receiving, during initialization of the transceiver, a message indicating how the shared memory is to be used by the interleaver or the deinterleaver.

11. The transceiver of claim **10**, further comprising:

an allocation module designed to allocate the shared memory based on one or more communication parameters.

12. The transceiver of claim **11**, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a Bit Error Rate (BER).

13. The transceiver of claim **10**, wherein the transceiver is connected to a second transceiver using a wired or wireless channel and the transceivers are used to transport video, internet access and voice data.

14. The transceiver of claim **10**, wherein the transceiver is located in a linecard that is capable of transporting video.

15. The transceiver of claim **10**, wherein the transceiver is located in a customer premises modem that is capable of transporting video.

16. The transceiver of claim **10**, further comprising a shared processing module designed to provide processing resources to a plurality of coding and/or decoding modules.

17. The transceiver of claim **10**, wherein the transceiver includes at least one digital signal processor.

18. The transceiver of claim **10**, wherein the transceiver includes at least one ASIC.

19. An apparatus comprising:

a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path, the multicarrier communications transceiver being associated with a memory,

wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

20. The apparatus of claim **19**, wherein the message is based on one or more communication parameters.

21. The apparatus of claim **20**, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

22. The apparatus of claim **19**, wherein the transceiver is configured to transport video, internet access and voice data using a wired or wireless channel.

23. The apparatus of claim **19**, wherein the apparatus is a customer premises modem that is capable of transporting video.

24. The apparatus of claim **19**, wherein the transceiver includes a shared processing module configured to provide processing resources to a plurality of coding and/or decoding modules.

25. The apparatus of claim **19**, wherein the transceiver includes at least one digital signal processor.

26. The apparatus of claim **19**, wherein the transceiver includes at least one ASIC.

27. The apparatus of claim **19**, wherein a sum of a maximum amount of the memory that can be allocated to the interleaving function and a maximum amount of the memory that can be allocated to the deinterleaving function is more than a total amount of the memory.

28. An apparatus comprising:

a multicarrier communications transceiver that is configured to generate a message during an initialization of the transceiver, perform an interleaving function associated with a first latency path, and perform a deinterleaving function associated with a second latency path, the transceiver being associated with a memory,

wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time and wherein the generated message indicates how the memory has been allocated between the interleaving function and the deinterleaving function.

29. The apparatus of claim **28**, wherein the message is based on one or more communication parameters.

30. The apparatus of claim **29**, wherein at least one of the communication parameters is a data rate, a latency, an INP value, or a Bit Error Rate (BER).

31. The apparatus of claim **28**, wherein the transceiver is configured to transport video, internet access and voice data using a wired or wireless channel.

32. The apparatus of claim **28**, wherein the apparatus is a linecard that is capable of transporting video.

33. The apparatus of claim **28**, wherein the transceiver includes a shared processing module configured to provide processing resources to a plurality of coding and/or decoding modules.

34. The apparatus of claim **28**, wherein the transceiver includes at least one digital signal processor.

35. The apparatus of claim **28**, wherein the transceiver includes at least one ASIC.

36. The apparatus of claim **28**, wherein a sum of a maximum amount of the memory that can be allocated to the interleaving function and a maximum amount of the memory that can be allocated to the deinterleaving function is more than a total amount of the memory.

37. A method of operating components of a telecommunications network, the components including a first multicarrier communications transceiver located in a linecard and a second multicarrier communications transceiver located at a customer premises, the first transceiver being configured to perform a first interleaving function associated with a first latency path and perform a first deinterleaving function associated with a second latency path, the second transceiver being configured to perform a second deinterleaving function associated with the first latency path and perform a second interleaving function associated with the second latency path and each of the first and second transceivers being associated with a respective memory, the method comprising:

causing the first transceiver to allocate the memory associated with the first transceiver between the first interleaving function performed by the first transceiver and the first deinterleaving function performed by the first transceiver, wherein at least a portion of the memory associated with the first transceiver may be allocated to the first interleaving function performed by the first

transceiver or the first deinterleaving function performed by the first transceiver at any one particular time; and

causing the first transceiver to transmit a message to the second transceiver during an initialization of the second transceiver, wherein the message indicates how the memory associated with the second transceiver is to be allocated between the second interleaving function performed by the second transceiver and the second deinterleaving function performed by the second transceiver and wherein at least a portion of the memory associated with the second transceiver may be allocated to the second interleaving function performed by the second transceiver or the second deinterleaving function performed by the second transceiver at any one particular time depending on the message.

38. The method of claim **37**, wherein the message is transmitted or received using a wired or wireless channel and wherein the method further comprises causing the first transceiver to transport video, internet access and voice data using the wired or wireless channel.

39. The method of claim **37**, further comprising allocating a shared processing module to a plurality of coding and/or decoding modules within the first transceiver.

40. The method of claim **37**, wherein the message is based on one or more communication parameters.

41. The method of claim **40**, wherein at least one of the communication parameters is a data rate, a latency, an INP value or a bit error rate (BER).

42. The method of claim **37**, wherein the telecommunications network is a DSL network.

43. The method of claim **37**, wherein the first transceiver is included within a line card.

44. The method of claim **37**, wherein the second transceiver is included within a customer premises modem.

45. The method of claim **37**, wherein a sum of a maximum amount of the memory associated with the first transceiver that can be allocated to the first interleaving function performed by the first transceiver and a maximum amount of the memory associated with the first transceiver that can be allocated to the deinterleaving function performed by the first transceiver is more than a total amount of the memory associated with the first transceiver.

46. The method of claim **37**, wherein a sum of a maximum amount of the memory associated with the second transceiver that can be allocated to the second interleaving function performed by the second transceiver and a maximum amount of the memory associated with the second transceiver that can be allocated to the deinterleaving function performed by the second transceiver is more than a total amount of the memory associated with the second transceiver.

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EXHIBIT 6

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC. Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC. and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC. Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC, Plaintiff, v. TQ DELTA, LLC. Defendant.	Civil Action No. 15-cv-121-RGA

[PROPOSED] CLAIM CONSTRUCTION ORDER FOR FAMILY 3 PATENTS

The Court has determined that the terms below shall be given the following meaning for U.S. Patent Nos. 7,831,890 ("the '890 patent"), 7,836,381 ("the '381 patent"), 7,844,882 ("the '882 patent"), 8,276,048 ("the '048 patent"), 8,495,473 ("the '473 patent"), and 8,607,126 ("the '126 patent"):[1]

1. **"shared memory"** – "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"

2. **"amount of memory"** – plain meaning

3. **"the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]"** – "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"

4. **"latency path"** – "transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay"

5. **"wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message"** – plain meaning

6. **"portion of memory"** – plain meaning

7. **"memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function"** – "an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"

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[1] The Court has not announced a meaning for the term "transceiver."

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8. "wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second] deinterleaving function" – "wherein the generated message indicates the amount of memory that has been allocated to the [first deinterleaving / interleaving] function and the amount of memory allocated to the [second] deinterleaving function"

IT IS SO ORDERED this 28 day of December, 2017.

Richard G. Andrews
The Honorable Richard G. Andrews

EXHIBIT 7

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC. Defendant.	Civil Action No. 13-cv-1835-RGA
TQ DELTA, LLC, Plaintiff, v. ZYXEL COMMUNICATIONS, INC. and ZYXEL COMMUNICATIONS CORPORATION, Defendants.	Civil Action No. 13-cv-2013-RGA
TQ DELTA, LLC, Plaintiff, v. ADTRAN, INC. Defendant.	Civil Action No. 14-cv-954-RGA
ADTRAN, INC, Plaintiff, v. TQ DELTA, LLC. Defendant.	Civil Action No. 15-cv-121-RGA

~~[PROPOSED]~~ CLAIM CONSTRUCTION ORDER FOR FAMILY 1 PATENTS

The Court has determined that the terms below shall be given the following meaning for U.S. Patent No. 7,889,784 ("the '784 patent"):

1. **"transceiver"** – "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"

2. **"test information"** – "information relating to a characteristic of a communication channel or the communications equipment operating on that channel"

3. **"Showtime"** – "the state of the transceiver reached after all initialization and training is completed, in which user data is transmitted or received"

4. **"array representing Signal to Noise ratio per subchannel during Showtime information"** – "ordered set of values representative of the signal to noise ratio of respective subchannels during the state of the transceiver reached after all initialization and training is completed, in which user data is transmitted or received"

5. **"multicarrier"** – "having multiple carrier signals that are combined to produce a transmission signal"

6. **"subchannel"** – "range within the frequency band of a multicarrier communications channel, wherein the range is associated with a single carrier signal."

IT IS SO ORDERED this 6 day of February, 2018.

The Honorable Richard G. Andrews

EXHIBIT 8

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff/Counterdefendant, v. 2WIRE, INC. Defendant/Counterclaimant.	Civil Action No. 13-1835-RGA **JURY TRIAL DEMANDED**

DEFENDANT 2WIRE, INC.'S INVALIDITY CONTENTIONS IN RESPONSE TO TQ DELTA'S JULY 2, 2018 FINAL INFRINGEMENT CONTENTIONS

Pursuant to the Court's April 11, 2018 Final Scheduling Order, defendant 2Wire, Inc. ("2Wire") provides the following invalidity contentions in response to TQ Delta's Final Claim Charts for Products that Contain Broadcom DSL Chips, served on July 2, 2018.[1]

I. PRELIMINARY STATEMENT

In its Final Claim Charts for Products that Contain Broadcom DSL Chips, served on July 2, 2018, TQ Delta identified, and 2Wire provides its invalidity contentions for, the following claims:

- Family 1: U.S. Patent No. 7,889,784 (the "'784 Patent") claims 1 and 2 (collectively, the "Family 1 Patent" and the "Asserted Family 1 Claims");
- Family 2: U.S. Patent No. 7,453,881 (the "'881 Patent") claims 17 and 18 (collectively, the "Family 2 Patent" and the "Asserted Family 2 Claims");

[1] TQ Delta identified the asserted claims for each of the patent families in its in its Final Claim Charts for Products that Contain Broadcom DSL Chips, served on July 2, 2018. We collectively refer to those asserted claims here as "TQ Delta Asserted Claims".

- Family 3: U.S. Patent No. 8,276,048 (the "'048 Patent") claim 1, U.S. Patent No. 7.385,381 (the "'381 Patent") claim 5, U.S. Patent No. 7,844,882 (the "'882 Patent") claim 13 and U.S. Patent No. 8,495,473 (the "'473 Patent") claim 19 (collectively, the "Family 3 Patents" and the "Asserted Family 3 Claims");
- Family 4: U.S. Patent No. 7292,627 (the "'627 Patent") claim 26, U.S. Patent No. 8,073,041 (the "'041 Patent") claim 14, and U.S. Patent No. 8,909,008 (the "'008 Patent") claim 14 (collectively, the "Family 4 Patents" and the "Asserted Family 4 Claims");
- Family 5: U.S. Patent No. 7,451,379 (the "'379 Patent") claims 11 and 16 and U.S. Patent No. 8,516,337 (the "'337 Patent") claims 10 and 16 (collectively, the "Family 5 Patents" and the "Asserted Family 5 Claims");
- Family 6: U.S. Patent No. 8,462,835 (the "'835 Patent") claims 8 and 10 (collectively, the "Asserted Family 6 Claims").

2Wire's invalidity contentions are responsive only to the contentions and charts provided on July 2, 2018 by TQ Delta in its Final Claim Charts for Products that Contain Broadcom DSL Chips. 2Wire does not waive, and explicitly reserves all rights to assert, any and all invalidity contentions and arguments (including but not limited to contentions and arguments disclosed herein) with regard to any other claims on infringement contentions that TQ Delta may be permitted to assert in this case or otherwise.

2Wire's search for, and analysis of, prior art is ongoing, and 2Wire continues to investigate the public use, sale, or offer for sale of products and systems that may anticipate or render obvious one or more of TQ Delta's Asserted Claims. 2Wire also continues to investigate and analyze TQ Delta's Asserted Claims and to develop new bases and grounds for invalidity.

2Wire reserves the right to supplement and/or amend its contentions once it has been afforded an opportunity to conduct discovery with regard to the invalidity of TQ Delta's Asserted Claims.

Moreover, the Court has not yet entered a claim construction order on Family 5 in this case. Accordingly, 2Wire thus reserves the right to modify, amend, or supplement its invalidity contentions as may be necessary or appropriate following the entry of a claim construction order on Family 5 in particular in this case.

Prior art not included here, whether known or unknown to 2Wire, may become relevant. In particular, 2Wire is currently unaware of the extent to which TQ Delta will contend that limitations of TQ Delta's Asserted Claims are not disclosed in the prior art identified by 2Wire. To the extent that such issues arise, 2Wire reserves the right to identify other prior art references that would disclose, teach, suggest, practice, or render obvious the allegedly missing limitations.

2Wire's invalidity claim charts (Exhibits A-1 through M-8) cite to particular teachings and disclosures of the prior art as applied to TQ Delta's Asserted Claims. 2Wire's citations are intended to generally disclose the grounds for its invalidity contentions – not to provide an exhaustive list of supporting evidence. Moreover, persons of ordinary skill in the art may view an item of prior art in the context of other publications, literature, products, and understanding. Thus, the cited portions are only examples, and 2Wire reserves the right to rely on uncited portions of the prior art references and on other publications and expert testimony as aids in understanding and interpreting the cited portions as additional evidence that the prior art discloses a claim limitation or the claimed invention as a whole or as evidence of the obviousness based on, among other things, contemporaneous development by others. 2Wire further reserves the right to rely on uncited portions of the prior art references, other publications, and testimony (including expert testimony) to establish bases for anticipation or

combinations of certain prior art references that render TQ Delta's Asserted Claims obvious. Additionally, citations to a particular figure in a reference include the caption and description of the figure and any text relating to the figure. Similarly, citations to particular text referring to a figure include the figure and caption as well.

These invalidity contentions are based on 2Wire's current understanding of TQ Delta's Asserted Claims, and TQ Delta's apparent interpretation of those claims, to the extent that can be divined from TQ Delta's Final Claim Charts for Products that Contain Broadcom DSL Chips, served on July 2, 2018. Thus, these invalidity contentions, including the attached charts, may reflect alternative positions as to claim construction and scope. By including prior art that would anticipate or render obvious TQ Delta's Asserted Claims based on TQ Delta's apparent constructions or on any other particular construction, 2Wire is neither adopting such constructions nor admitting their accuracy. Nothing herein should be construed as an admission that 2Wire agrees with TQ Delta's apparent interpretation of the scope of claim language. 2Wire reserves the right to challenge TQ Delta's implicit constructions as inconsistent with the Court's claim construction rulings, or on other grounds. Similarly, nothing herein shall be construed as an admission regarding the application of the asserted claims to any of 2Wire's accused products.

Because TQ Delta has now provided its final infringement contentions with respect to Broadcom products, TQ Delta should not be permitted to change or amend its contentions, and 2Wire reserves the right to object to any attempt by TQ Delta to change or amend its contentions. Should TQ Delta be permitted to further amend its infringement contentions, or to provide additional information on infringement and TQ Delta's apparent construction of the asserted

claims, 2Wire reserves the right to amend and supplement these invalidity contentions as appropriate.

Finally, 2Wire does not waive, and expressly reasserts here, the grounds for invalidity set out in its preliminary invalidity contentions served on September 24, 2015 and its supplemental invalidity contentions served on January 23, 2017.

II. INVALIDITY CONTENTIONS FOR PATENT FAMILY 1

A. Invalidity Under 35 U.S.C. § 101

TQ Delta's Asserted Family 1 Claims are invalid for failing to recite patentable subject matter under 35 U.S.C. § 101. Section 101 provides that "[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title." Nonetheless, there are three recognized exceptions to Section 101: "laws of nature, physical phenomena, and abstract ideas." *Bilski v. Kappos*, 561 U.S. 593, 601 (2010) (*quoting Diamond v. Chakrabarty*, 447 U.S. 303, 309 (1980)).

TQ Delta's Asserted Family 1 Claims are invalid for claiming no more than an abstract idea. In *Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014), the Supreme Court set out a two-part test for determining whether a claim recites patent-eligible subject matter. First, the court must determine whether the claims at issue are directed toward laws of nature, natural phenomena, or abstract ideas. *Id.* at 2355. Second, if the claims are directed toward ineligible subject matter, the court must then consider the claim elements – both individually and as an ordered combination – to determine whether they add an "inventive concept." *Id.* Merely claiming a generic "computer" to implement an abstract idea is not sufficient to transform the computer into a patent-eligible invention. *Id.* at 2357-50.

Here, claims 1 and 2 of the '784 Patent claim nothing more than the abstract idea of

measuring diagnostic information and communicating it to a connected device. More specifically, the Asserted Claims claim the abstract idea of collecting diagnostic or test information regarding the status of remote DSL subscriber equipment. Collecting diagnostic information is a long standing engineering practice and is well known in many fields of engineering. The communication of such information is similarly long standing and well known. The claims are untethered to any specific implementation or environment.

Nor do the elements of the claims – whether individually or as a whole – evidence any "inventive concept." The concept of signal-to-noise ratio in communication channels was well known, as was the need to communicate that information. The claims recite only a conventional technological environment, such as a conventional transceiver, and conventional methods of communicating information, that were well-known at the time of the alleged invention. Moreover, the '784 Patent claims does not require the transceiver to do anything with the message, or the diagnostic or test information within the message. For example, the '784 Patent claims do not require processing the message, interpreting the information in the message, or taking any action based on the information in the message. Accordingly, claims 1 and 2 of the '784 Patent are invalid for failure to recite patentable subject matter.

Defendant hereby incorporates in its entirety the briefing on its Motion for Judgment on the Pleadings and all declarations in support (D.I. 250, 251, 259), in which 2Wire argued that the claims of the Family 1 patent, including the '784 Patent, were invalid for failure to recite patentable subject matter under 35 U.S.C. § 101. 2Wire's motion was denied in an order dated February 6, 2017 (D.I. 266). Defendant reserves the right to raise the issue of whether the '784 Patent recites patentable subject matter on summary judgment and/or at trial. By way of example, there may be issues of fact relating to whether elements of the asserted claims are well-

understood, routine and conventional to one of ordinary skill in the art. *See, e.g., Berkheimer v. HP Inc.*, 881 F.3d 1360, 1368 (Fed. Cir. 2018) ("The question of whether a claim element or combination of elements is well-understood, routine and conventional to a skilled artisan in the relevant field is a question of fact."); *Aatrix Software, Inc. v. Green Shades Software, Inc.*, 882 F.3d 1121, 1128 (Fed. Cir. 2018) ("While the ultimate determination of eligibility under § 101 is a question of law, like many legal questions, there can be subsidiary fact questions which must be resolved en route to the ultimate legal determination.").

B. Collateral Estoppel

TQ Delta is estopped from asserting claims 1 and 2 of the ’784 Patent in view of decisions rendered by the Patent Trial and Appeal Board in IPR2016-01007 and other proceedings, and in view of positions taken by TQ Delta in that proceeding. In IPR2016-01007, the PTAB cancelled all challenged claims of U.S. Patent No. 8,432,956, including claim 9 of the ’956 Patent, which is substantively identical to and contains the same limitations as claims 1 and 2 of the ’784 Patent. The ’956 Patent claims priority to the same provisional application as the ’784 Patent. Here, the identical issue was previously adjudicated by the PTAB, the issue of invalidity of those claim elements was actually litigated, the previous determination was necessary to the PTAB’s decision to cancel all claims, and TQ Delta was fully represented in the prior action at the PTAB. *See Jean Alexander Cosmetics, Inc. v. L’Oreal USA, Inc.*, 458 F.3d 244, 249 (3d Cir. 2006). TQ Delta is precluded from arguing that claims 1 and 2 of the ’784 Patent are valid. *See, e.g., MaxLinear, Inc. v. CF CRESPE LLC*, 880 F.3d 1373, 1376 (Fed. Cir. 2018) (holding that patent claims found invalid in prior IPRs were subject to collateral estoppel in subsequent PTAB proceedings).

C. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

Claims 1 and 2 of the ’784 Patent are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 6,445,730 (“Greszczuk”)
- U.S. Patent No. 6,631,120 (“Milbrandt”)
- U.S. Patent No. 6,636,603 (“Milbrandt 603”)
- U.S. Patent No. 6,606,719 (“Ryckebusch”)
- U.S. Patent No. 6,434,119 (“Wiese”)
- U.S. Patent No. 6,865,232 (“Isaksson”)
- U.S. Patent No. 6,219,378 (“Wu”)
- U.S. Patent No. 4,679,227 (“Hughes-Hartogs”)
- U.S. Patent No. 6,788,705 (“Rango”)
- ANSI T1.413-1998, “Network and Customer Installation Interfactes – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface”
- ITU-T Recommendation G.992.1, “Asymmetric Digital Subscriber Line (ADSL) Transceivers”
- The Telebit T2500 Reference Manual (“T2500”)

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits A-1 through A-16 demonstrate how TQ Delta’s Asserted Family 1 Claims are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the ’784 Patent and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire reserves the right to assert that any claim element is disclosed

in other portions of the cited references. In addition, 2Wire identifies, and incorporates here by reference, all prior art of record in the prosecution history of the ’784 Patent (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports, or specifications), any of which may anticipate and/or render TQ Delta’s Asserted Family 1 Claims obvious. Further, 2Wire identifies any TQ Delta patents that claim the same priority date as the ’784 Patent and disclose the same subject matter and for which a terminal disclaimer was not filed during prosecution, under the doctrine of obviousness-type double patenting. Additional evidence regarding the features and elements of prior art references may be provided by witness testimony, or by additional documents and materials describing the prior art, that may be identified through the course of ongoing discovery and investigation.

To the extent that a reference above is found to be missing a limitation of TQ Delta’s Asserted Claims, any one of the prior art references identified above may be combined with any one or more of the other references identified above and the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render TQ Delta’s Asserted Claims obvious under 35 U.S.C. § 103:

- U.S. Patent No. 6,590,893 (“Hwang”)
- U.S. Patent No. 6,366,644 (“Sisk”)
- U.S. Patent No. 4,438,551 (“Baran”)
- U.S. Patent No. 5,838,268 (“Frenkel”)
- U.S. Patent No. 4,679,227 (“Hughes-Hartogs”)
- U.S. Patent No. 6,606,719 (“Ryckebusch”)
- U.S. Patent No. 6,219,378 (“Wu”)

- ANSI T1.413-1995, "Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface"
- ANSI T1.413-1998, "Network and Customer Installation Interfactes – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface"
- Gilbert Held, Data Communications Networking Devices: Operation, Utilization and LAN and WAN Internetworking, 4th edition

Specific combinations that render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103 using these references are set forth in Exhibits A-1 through A-16. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the '784 Patent (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports or specifications), to render TQ Delta's Asserted Family 1 Claims obvious. Further, any of the foregoing anticipatory or secondary prior art listed above may be combined with one another to render TQ Delta's Asserted Family 1 Claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or more of the prior art references identified above to arrive at the combination of elements recited in each of TQ Delta's Asserted Claims. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field, high-speed communications and DSL. In addition, it would have been obvious to try combining the prior art

references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results. For example, those in the DSL and high-speed telecommunications industry had long understood the need to avoid sending a technician to diagnose problems with a subscriber line. Those in the industry also understood the benefits of being able to obtain information about a subscriber line remotely, without the necessity of sending out a technician. The motivation to combine references is exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire's invalidity charts and expert report(s) on invalidity.

To the extent that TQ Delta raises any secondary considerations of non-obviousness, for

example, in its expert reports, 2Wire reserves the right to address any such considerations, including by taking discovery on those issues and supplementing and/or amending its invalidity contentions.

In addition, the asserted claims of the ’784 Patent are invalid under the printed matter doctrine because certain limitations claim printed matter (i.e., content of information) that is not functionally or structurally related to the medium containing the printed matter. In the alternative, the asserted claims of the ’784 Patent are invalid under the printed matter doctrine because certain limitations claim printed matter and are not entitled to patentable weight, without which the claims are anticipated or rendered obvious by the cited references.

2Wire does not presently have any disclosures under 35 U.S.C. § 102(f). 2Wire reserves the right to amend and supplement these § 102(f) contentions as further information and discovery are obtained including, in particular, with regard to the alleged conception and reduction-to-practice of the patents-in-suit.

D. Invalidity Under 35 U.S.C. § 112

2Wire lists below exemplary grounds upon which it contends TQ Delta’s Asserted Family 1 Claims are invalid for failure to meet one or more requirements of 35 U.S.C. § 112. A more detailed basis for 2Wire’s written description, enablement, and indefiniteness defenses will be set forth in 2Wire’s expert report(s) on invalidity. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112 in light of discovery on invalidity issues and on any other basis permitted by the Court or the applicable rules. Such supplementation and/or amendments may include, but are not limited to, invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement.

Invalidity Under 35 U.S.C. § 112 ¶ 1: TQ Delta’s Asserted Family 1 Claims are invalid because the patent specification does not include sufficient description of the subject matter

claimed, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the allegedly claimed invention without undue experimentation. 2Wire further contends that the full scope of each asserted claim was not described with particularity in the specification to which priority is apparently sought, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "wherein bits in the message are modulated onto DMT symbols using Quadrature Amplitude Modulation (QAM) with more than 1 bit per subchannel" ('784 Patent, claims 1 and 2)
- "wherein at least one data variable of the one or more data variables comprises an array representing Signal to Noise ratio per subchannel during Showtime information" ('784 Patent, claims 1 and 2)

TQ Delta's Asserted Family 1 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

The accused products do not infringe TQ Delta's Asserted Family 1 Claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire, 2Wire's Interrogatory Responses, and any supplements thereto. To the extent TQ Delta's Asserted Family 1 Claims may eventually be construed so broadly as to cover the accused products, such a construction would render TQ Delta's Asserted Family 1 Claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: TQ Delta's Asserted Family 1 Claims are also invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed (i.e., the claims are indefinite). 2Wire contends that a person of ordinary skill in the art to which the purported invention pertains would not understand the scope of each asserted claim when read in light of the specification. By way of example, and without limitation, at least the following claim terms are indefinite under Section 112:

- "a transmitter portion capable of transmitting a message, wherein the message comprises one or more data variables that represent the test information . . . wherein at least one data variable of the one or more data variables comprises an array representing Signal to Noise ratio per subchannel during Showtime information" ('784 Patent, claim 1)
- "a receiver portion capable of receiving a message, wherein the message comprises one or more data variables that represent the test information . . . wherein at least one data variable of the one or more data variables comprises an array representing Signal to Noise ratio per subchannel during Showtime information" ('784 Patent, claim 2)
- "wherein bits in the message are modulated onto DMT symbols using Quadrature Amplitude Modulation (QAM) with more than 1 bit per subchannel" ('784 Patent, claims 1 and 2)

TQ Delta's Asserted Family 1 Claims (and all other claims in the asserted patent that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regarded as their invention.

Further, TQ Delta's Asserted Family 1 Claims are invalid under Section 112 because they purport to claim both an apparatus and a method of using the apparatus. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). To the extent that TQ Delta's Asserted Family 1 Claims do not invoke 35 U.S.C. § 112, ¶ 6 (pre-AIA), those claims are invalid for merely claiming the function of an apparatus. Thus, each asserted claim is invalid as indefinite under Section 112, paragraph 2.

III. INVALIDITY CONTENTIONS FOR PATENT FAMILY 2

A. Invalidity Under 35 U.S.C. § 101

TQ Delta's Asserted Family 2 Claims are invalid for failing to recite patentable subject matter under 35 U.S.C. § 101. Section 101 provides that "[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title." Nonetheless, there are three recognized exceptions to Section 101: "laws of nature, physical phenomena, and abstract ideas." *Bilski v. Kappos*, 561 U.S. 593, 601 (2010) (*quoting Diamond v. Chakrabarty*, 447 U.S. 303, 309 (1980)).

TQ Delta's Asserted Family 2 Claims are invalid for claiming no more than an abstract idea. In *Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014), the Supreme Court set out a two-part test for determining whether a claim recites patent-eligible subject matter. First, the court must determine whether the claims at issue are directed toward laws of nature, natural phenomena, or abstract ideas. *Id.* at 2355. Second, if the claims are directed toward ineligible subject matter, the court must then consider the claim elements – both individually and as an ordered combination – to determine whether they add an "inventive concept." *Id.* Merely claiming a generic "computer" to implement an abstract idea is not sufficient to transform the computer into a patent-eligible invention. *Id.* at 2357-50.

Here, claims 17-18 of the ’881 Patent recite nothing more than the abstract idea of reducing delay by, for example, speeding one connection up or slowing another connection down. More specifically, the referenced claims (and all claims of the Family 2 Patent) claim the abstract idea of reducing a difference in latency (arrival time) between information carried over two communication paths by either increasing the rate at which information is carried and processed over one path or decreasing the rate at which information is carried and processed over the other path. Increasing or decreasing the rate over which information is carried over a communication path, or increasing and decreasing the rate at which data is processed, are long standing engineering practices and are well known in many fields outside of engineering, such as sending messages by post or hand delivery, for delivery within a particular time frame or by a particular date. The claims are untethered to any specific implementation or environment, and the patents and specification do not limit the concept of reducing a difference in delay. Moreover, the claims’ recitation of “a plurality of bonded transceivers” does not provide sufficient structure to render these claims non-abstract.

Nor do the elements of the claims – whether individually or as a whole – evidence any “inventive concept.” The concept of latency in communication paths was well understood, routine and conventional to one of ordinary skill in the art, as was the need to reduce latency between communication paths to keep messages or parts of messages from being received too far apart in time. All of the “transmission parameters” cited in the claims likewise were parameters well-understood to increase or decrease delay, or latency, (depending on whether the parameters were increased or decreased) both on individual communication paths and as between multiple communication paths. The use of such “transmission parameters” to increase or decrease delay was well-understood, routine and conventional to one of ordinary skill in the art at the time of the

alleged invention.

B. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

Claims 17-18 of the ’881 Patent (the “Family 2 Patent”) are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 6,222,858 (“Counterman”)
- U.S. Patent No. 6,178,448 (“Gray”)
- U.S. Patent No. 7,068,657 (“Keller-Tuberg”)
- PCT Application No. PCT/NO99/0024, WO 99/39468 (“Edvardsen”)
- ATM Forum Technical Committee, Inverse Multiplexing over ATM (IMA) Specification Version 1.0 (“IMA Spec 1.0”)

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits B-1 through B-5 demonstrate how TQ Delta’s Asserted Claims of the Family 2 Patent are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the Family 2 Patent and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire reserves the right to assert that any claim element is disclosed in other portions of the cited references. In addition, 2Wire identifies, and incorporates here by reference, all prior art of record in the prosecution history of the Family 2 Patent (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports, or specifications), any of which may anticipate and/or render TQ Delta’s Asserted Claims obvious. Further, 2Wire identifies any TQ Delta patents that claim the same

priority date as any of the Family 2 Patents and disclose the same subject matter and for which a terminal disclaimer was not filed during prosecution, under the doctrine of obviousness-type double patenting. Additional evidence regarding the features and elements of prior art references may be provided by witness testimony, or by additional documents and materials describing the prior art, that may be identified through the course of ongoing discovery and investigation.

To the extent that a reference above is found to be missing a limitation of TQ Delta's Asserted Claims, any one of the prior art references identified above may be combined with any one or more of the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103:

- U.S. Patent No. 5,617,417 ("Sathe")
- U.S. Patent No. 6,822,960 ("Manchester")
- U.S. Patent No. 5,617,417 ("Sathe")
- U.S. Patent No. 5,608,733 ("Valee '733")
- U.S. Patent No. 6,680,954 ("Cam")
- U.S. Patent No. 6,205,142 ("Vallee '142")
- U.S. Patent No. 5,727,051 ("Holender")
- U.S. Patent No. 6,178,448 ("Gray")
- U.S. Patent No. 6,408,005 ("Fan")
- U.S. Patent No. 6,941,252 ("Nelson")
- U.S. Patent No. 6,775,268 ("Wang '268")

- U.S. Patent No. 6,396,837 ("Wang '837")
- U.S. Patent No. 6,747,964 ("Bender")
- U.S. Patent No. 6,002,670 ("Rahman")
- U.S. Patent No. 7,343,543 ("Mantha")
- U.S. Patent No. 6,775,320 ("Tzannes '320")
- U.S. Patent No. 6,772,388 ("Cooper")
- U.S. Patent No. 6,956,872 ("Djokovic")
- EP1009154 (A2) ("Aravamudan")
- DSL Forum Recommendation TR-042
- ITU-T Recommendation G.992.1 (06/1999)
- Broadband Forum Recommendation TR-042

Specific combinations that render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103 using these references are set forth in Exhibits B-1 through B-5. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the Family 2 Patent (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports or specifications), to render TQ Delta's Asserted Claims obvious. Further, any of the foregoing anticipatory or secondary prior art listed above may be combined with one another to render TQ Delta's Asserted Claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or

more of the prior art references identified above to arrive at the combination of elements recited in each of TQ Delta's Asserted Claims. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field, high-speed communications, and more specifically, ATM and DSL networks. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results. For example, one common, known method of handling a difference in delay was to provide an additional buffer or memory of appropriate size. Those in the DSL and high-speed communications industry understood that larger memory increased costs and complexity

of a transceiver or modem, and that a smaller, cheaper, less complex device was desirable. Moreover, those of ordinary skill in the art at the time of the alleged invention understood that increased differential delay in multiplexed (or "bonded") communications systems had the effect of slowing down overall data rates. Those of ordinary skill in the art also understood that providing higher overall data rates was desirable and could provide an advantage in the marketplace. The motivation to combine references is exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire's attached invalidity charts and expert report(s) on invalidity following claim construction and discovery on validity issues.

To the extent that TQ Delta raises any secondary considerations of non-obviousness, for example, in its expert reports, 2Wire reserves the right to address any such considerations.

C. Invalidity Under 35 U.S.C. § 112

2Wire lists below exemplary grounds upon which it contends TQ Delta's Asserted Claims are invalid for failure to meet one or more requirements of 35 U.S.C. § 112. A more detailed basis for 2Wire's written description, enablement, and indefiniteness defenses will be set forth in 2Wire's expert report(s) on invalidity. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112 in light of discovery on invalidity issues and on any other basis permitted by the Court or the applicable rules. Such supplementation and/or amendments may include, but are not limited to, invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement.

Invalidity Under 35 U.S.C. § 112 ¶ 1: TQ Delta's Asserted Family 2 Claims are invalid because the patent specification does not include sufficient description of the subject

matterclaimed, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the claimed subject matter without undue experimentation. 2Wire further contends that the full scope of each asserted claim was not described with particularity in the specification to which priority is apparently sought, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "utilizing at least one transmission parameter value to reduce a difference in latency" ('881 Patent, claims 17, 18)
- "bonded transceivers" ('881 Patent, claims 17, 18)
- "A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers" ('881 Patent, claims 17, 18)

TQ Delta's Asserted Family 2 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

The accused products do not infringe TQ Delta's Asserted Family 2 Claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire, its Interrogatory Responses, and any supplements thereto. To the extent TQ Delta's Asserted Claims may eventually be construed so broadly as to cover the accused products, such a construction would render TQ Delta's Asserted Claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: TQ Delta's Asserted Family 2 Claims are also invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed (i.e., the claims are indefinite). A person of ordinary skill in the art to which the purported invention pertains would not understand the scope of each asserted claim when read in light of the specification. By way of example, and without limitation, at least the following claim terms are indefinite under Section 112:

- "utilizing at least one transmission parameter value to reduce a difference in latency" ('881 Patent, claims 17, 18)
- "bonded transceivers" ('881 Patent, claims 17, 18)
- "reduce a difference in latency" ('881 Patent, claims 17, 18)
- "A plurality of bonded transceivers, each bonded transceiver utilizing at least one transmission parameter value to reduce a difference in latency between the bonded transceivers" ('881 Patent, claims 17, 18)

TQ Delta's Asserted Family 2 Claims (and all other claims in the asserted patent that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regarded as their invention.

Further, TQ Delta's Asserted Family 2 Claims are invalid under Section 112 because they purport to claim both an apparatus and a method of using the apparatus. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). To the extent that TQ Delta's Asserted Claims do not invoke 35 U.S.C. § 112, ¶ 6 (pre-AIA), those claims are invalid for merely claiming the function of an apparatus. Thus, each asserted claim is invalid as indefinite under Section 112, paragraph 2.

IV. INVALIDITY CONTENTIONS FOR PATENT FAMILY 3

A. Invalidity Under 35 U.S.C. § 101

TQ Delta's Asserted Family 3 Claims are invalid for failing to recite patentable subject matter under 35 U.S.C. § 101. Section 101 provides that "[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title." Nonetheless, there are three recognized exceptions to Section 101: "laws of nature, physical phenomena, and abstract ideas." *Bilski v. Kappos*, 561 U.S. 593, 601 (2010) (*quoting Diamond v. Chakrabarty*, 447 U.S. 303, 309 (1980)).

TQ Delta's Asserted Family 3 Claims are invalid for claiming no more than an abstract idea. In *Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014), the Supreme Court set out a two-part test for determining whether a claim recites patent-eligible subject matter. First, the court must determine whether the claims at issue are directed toward laws of nature, natural phenomena, or abstract ideas. *Id.* at 2355. Second, if the claims are directed toward ineligible subject matter, the court must then consider the claim elements – both individually and as an ordered combination – to determine whether they add an "inventive concept." *Id.* Merely claiming a generic "computer" to implement an abstract idea is not sufficient to transform the computer into a patent-eligible invention. *Id.* at 2357-50.

Here, TQ Delta's Asserted Family 3 Claims are drawn to no more than the abstract idea of dividing a shared resource between two needs as instructed. Dividing resources according to needs is a long-standing practice in almost every human endeavor, both technological and social. For example, one might instruct an assistant to allocate space in filing cabinets to different cases depending on the rate at which information or materials are filed in one case versus the other. Nor do the elements of the claims – whether individually or as a whole – evidence any

"inventive concept." The claims are untethered to any specific implementation or environment, and the patents and specification do not limit the concept of allocating a shared resource.

The claims purport to relate to allocation of a shared memory between functions in a technological environment in accordance with an instruction or message, but the concept of allocation of memory between functions in accordance with an instruction is perhaps one of the most fundamental aspects of any general purpose computer processing system and is well known. *See, e.g.*, U.S. Pat. No. 4,827,406, issued May 2, 1989 to Bischoff et al., at col. 1:39-45 ("In one prior art system employing a main processor and a secondary processor (co-processor) sharing utilization of a single bus, the main processor, with the aid of an advanced operating system, allocated portions of a large, main memory to various devices, such as the co-processor, direct memory access controller (OMA), and other intelligent controllers."); *id.* at col. 1:64-2:2 ("It would, therefore, be highly advantageous to provide a large, common memory to be allocated in subdivisions, or pages, to each of a plurality of processors sharing a bus, without the necessity of utilizing a highly advanced operating system, or 'on-board', rigidly dedicated memory, individually associated with the each of the processors."); U.S. Patent No. 5,689,707 to Donnelly et al., at col. 1:16-18 ("Computer operating systems dynamically allocate memory in a computer system while executing programs, i.e., processes, to use for specific functions."); U.S. Pat. No. 5,159,681, issued Oct. 27, 1992 to Beck et al. at Abstract ("A memory management system for a page printer controller (11) which includes random access memory (17) allocated among bit map memory (30), page buffer memory (29), and user memory (28). The memory management system allocates the random access memory to provide either a large bit map memory or, responsive to needs of the controller (11) for increased memory for other uses, for allocating the random access memory (17) to provide a small bit map memory and place more

memory in the page buffer memory (29) and user memory (28).”). All recited elements of the apparatus (e.g., interleavers, deinterleavers, transceivers, shared memories) were staples of telecommunications in many fields including DSL communications, and even the exchange of messages to identify memory requirements for the recited functions was a well-known and necessary practice in DSL communications. *See, e.g.*, Exhibits C-4 and C-10, addressing U.S. Patent No. 6,707,822 to Fadavi-Ardekani et al. (“Fadavi-Ardekani”) in view of ITU-T Recommendation G.993.1 (6/2004) and in view of ITU-T Recommendation G.992.2 (1999). The only purported addition is the idea of allocating a shared resource as instructed, which is abstract and is not an inventive concept.

B. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

Claim 1 of the ’048 Patent, claims 19 of the ’473 Patent, claim 5 of the ’381 Patent, and claim 13 of the ’882 Patent (collectively, “Family 3 Patents”) are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 5,063,533 (“Erhart”)
- U.S. Patent Pub. No. 2005/0034046 (“Berkmann”)
- U.S. Patent No. 6,484,283 (“Stephen”)
- U.S. Patent No. 5,912,898 (“Khoury”)
- U.S. Patent No. 7,200,169 (“Suzuki”)
- U.S. Patent No. 6,775,320 (“Tzannes ’320”)
- U.S. Patent No. 6,381,728 (“Kang”)
- U.S. Patent No. 5,751,741 (“Voith”)
- U.S. Patent No. 7,269,208 (“Mazzoni”)
- U.S. Patent No. 6,707,822 to Fadavi-Ardekani et al. (“Fadavi-Ardekani”)
- ITU-T Recommendation G.993.1 (6/2004)

- ITU-T Recommendation G.992.1 (1999)
- ITU-T Recommendation G.992.2 (1999)
- ITU-T SG15/Q4 Contribution LB-031 ("LB-031")

In addition, the content of the Background section of the U.S. Patent No. 8,495,473 ("the '473 patent") is admitted prior art to the '473 Patent ("Admissions"). *See*, *e.g.*, '473 patent at col. 1:20-45.

Specific combinations that render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103 using these references are set forth in Exhibits C-1 through C-11, D-1 through D-25, E-1 through E-11, and F-1 through F-11. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits C-1 through C-11, D-1 through D-25, E-1 through E-11, and F-1 through F-11 demonstrate how TQ Delta's Asserted Family 3 Claims are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the Family 3 Patents and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire reserves the right to assert that any claim element is disclosed in other portions of the cited references. In addition, 2Wire identifies, and incorporates here by reference, all prior art of record in the prosecution history of the Family 3 Patents (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports, or specifications), any

of which may anticipate and/or render TQ Delta's Asserted Family 3 Claims obvious.

To the extent that a reference above is found to be missing a limitation of TQ Delta's Asserted Family 3 Claims, any one of the prior art references identified above may be combined with any one or more of the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render TQ Delta's Asserted Family 3 Claims obvious under 35 U.S.C. § 103:

- U.S. Patent Pub. No. 20030179770 ("Reznic")
- U.S. Patent Pub. No. 20050034046 ("Berkmann")
- U.S. Patent Pub. No. 20050254441 ("Levi")
- U.S. Patent Pub. No. 2003008821 ("Yokokawa")
- U.S. Patent Pub. No. 20030093750 ("Cameron")
- U.S. Patent Pub. No. 20010039637 ("Bengough")
- U.S. Patent No. 5063533 ("Erhart")
- U.S. Patent No. 5563915 ("Stewart")
- U.S. Patent No. 5751741 ("Voith")
- U.S. Patent No. 5757416 ("Birch")
- U.S. Patent No. 5867400 ("El-Ghoroury")
- U.S. Patent No. 5912898 ("Khoury")
- U.S. Patent No. 5968200 ("Amrany")
- U.S. Patent No. 5991857 ("Koetje")
- U.S. Patent No. 6151690 ("Peeters")
- U.S. Patent No. 6392572 ("Shiu")

- U.S. Patent No. 6480976 ("Pan")
- U.S. Patent No. 6484283 ("Stephen")
- U.S. Patent No. 6553534 ("Yonge")
- U.S. Patent No. 6704848 ("Song")
- U.S. Patent No. 6922444 ("Cai")
- U.S. Patent No. 6988234 ("Han")
- U.S. Patent No. 7187708 ("Shiu")
- U.S. Patent No. 7200169 ("Suzuki")
- U.S. Patent No. 7266132 ("Liu")
- U.S. Patent No. 7269208 ("Mazzoni")
- KR100295086B
- Eberle, *80-Mb/s QPSK and 72-Mb/s 64-QAM Flexible and Scalable Digital OFDM Transceiver ASICs for Wireless Local Area Networks in the 5-GHz Band*, IEEE Journal Of Solid-State Circuits, Vol. 36, No. 11, November 2001, p. 1829
- Texas Instruments, Inc., ITU-T SG15/Q4 Contribution LB-031, "VDSL2 – Constraining the Interleaver Complexity" ("LB-031")

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the Family 3 Patents (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports or specifications), to render TQ Delta's Asserted Family 3 Claims obvious. Further, any of the foregoing anticipatory or secondary prior art listed above may be combined with one another to render TQ Delta's Asserted Family 3 Claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or more of the prior art references identified above to arrive at the combination of elements recited in each of TQ Delta's Asserted Family 3 Claims. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field, high-speed communications and DSL systems. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combinations of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results. Those in the industry had long recognized that memory in a DSL (or other telecommunications) transceiver was a significant source of expense, complexity, and inefficiency. The benefits of

sharing memory between multiple processes or latency paths (for example, an interleaver and a deinterleaver) to reduce the amount of memory required in a system (and in turn, the cost) had also been recognized by those of ordinary skill in the art. Those of ordinary skill in the art had also recognized that allocating the ability to change the allocation of interleaver and deinterleaver memory would likewise be advantageous to further reduce the amount of memory required. The motivation to combine references is exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire's invalidity charts, and 2Wire's expert report(s) on invalidity.

There are no secondary considerations of non-obviousness pertinent to the obviousness of the subject matter of the asserted claims. To the extent that TQ Delta raises any secondary considerations of non-obviousness, for example, in its expert reports, 2Wire reserves the right to address any such considerations, including by taking discovery on those issues and supplementing and/or amending its invalidity contentions, as well as through 2Wire's expert report(s).

In addition, the asserted claims of Family 3 are invalid under the printed matter doctrine because certain limitations claim printed matter (i.e., content of information) that is not functionally or structurally related to the medium containing the printed matter. In the alternative, the asserted claims of Family 3 are invalid under the printed matter doctrine because certain limitations claim printed matter and are not entitled to patentable weight, without which the claims are anticipated or rendered obvious by the cited references. By way of example and

not of limitation, printed matter includes limitations directed to the contents of messages or data variables, such as a "message . . . specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" or that data bytes are "Reed Solomon (RS) coded data bytes."

Moreover, the Asserted Family 3 Claims are invalid to the extent that the named inventors did not themselves invent the subject matter sought to be patented. *See* 35 U.S.C. § 102(f). For example, named inventor Michael Lund testified that he did not recall to what extent he worked on the claimed subject matter of the Family 3 patents, and that he did not recall being involved in prosecution of the claimed subject matter of the Family 3 patents. *See* Transcript of Deposition of Michael A. Lund, Nov. 30, 2017 at *e.g.*, 67:8-74:7, 75:20-76:8, 79:21-80:13.

2Wire reserves the right to amend and supplement these § 102(f) contentions as further information and discovery are obtained including, in particular, with regard to the alleged conception and reduction-to-practice of the patents-in-suit.

C. Invalidity Under 35 U.S.C. § 112

2Wire lists below exemplary grounds upon which TQ Delta's Asserted Family 3 Claims are invalid for failure to meet one or more requirements of 35 U.S.C. § 112. A more detailed basis for 2Wire's written description, enablement, and indefiniteness defenses will be set forth in 2Wire's expert report(s) on invalidity. Furthermore, discovery regarding invalidity (e.g., inventor depositions, etc.) is ongoing. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112 in light of discovery on invalidity issues. Such supplementation and/or amendments may include, but are not limited to, and/or invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement should the claims be construed under 35 U.S.C. § 112 ¶ 6.

Invalidity Under 35 U.S.C. § 112 ¶ 1: TQ Delta's Asserted Family 3 Claims are invalid

because the patent specification does not include sufficient description of the claimed subject matter, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the claimed subject matter without undue experimentation. 2Wire further contends that the full scope of each of TQ Delta's Asserted Family 3 Claims was not described with particularity in the specification to which priority is apparently sought, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "a maximum number of bytes of memory that are available to be allocated" ('048 Patent, claim 1; '381 Patent, claim 5; '882 Patent, claim 13);
- "wherein the shared memory allocated to the [interleaver/deinterleaver] is used at the same time as the shared memory allocated to the [deinterleaver/interleaver]" ('048 Patent, claim 1; '381 Patent, claim 5; '882 Patent, claim 13);
- "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." ('473 Patent, claim 19)

TQ Delta's Asserted Family 3 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

2Wire's accused products do not infringe TQ Delta's Asserted Family 3 Claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire, and any supplements thereto. To the extent TQ Delta's Asserted Family 3 Claims may eventually be

construed so broadly as to cover the accused products, such a construction would render those claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: TQ Delta's Asserted Family 3 Claims are also invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed. 2Wire contends that a person of ordinary skill in the art to which the purported invention pertains would not understand the scope of each asserted claim when read in light of the specification. By way of example, and without limitation, at least the following claim terms are indefinite under Section 112:

- "a maximum number of bytes of memory that are available to be allocated" ('048 Patent, claim 1, '381 Patent, claim 5, '882 Patent, claim 13);
- "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver" ('048 Patent, claim 1, '381 Patent, claim 5, '882 Patent, claim 13);
- "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." ('473 Patent, claim 19)

TQ Delta's Asserted Family 3 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regard as their invention.

Further, TQ Delta's Asserted Family 3 Claims are invalid under Section 112. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). "*IPXL* indefiniteness arises when a person of ordinary skill in the art would be unable to tell if the apparatus itself

would infringe or if the apparatus would have to be used in a certain way to infringe." *Sound View Innovations, LLC v. Facebook, Inc*., No. 16-cv-116, 2017 WL 2221177, at *8 (D. Del. May 19, 2017) (Andrews, J.) (discussing *IPXL* 430 F.3d at 1384). Although *IPXL* addressed a claim that recited both an apparatus and method steps, the Federal Circuit recognized that the reason such claims are indefinite under section 112, paragraph 2 is that they are "not sufficiently precise to provide competitors with an accurate determination of the 'metes and bounds' of protection involved," making it unclear when infringement occurs. *IPXL,* 430 F.3d at 1384 (citation omitted). Thus, the focus of the inquiry is whether a person of ordinary skill in the art would know when infringement occurs, and whether the claim "does not apprise a person of ordinary skill in the art of its scope." *Id*. Moreover, after *IPXL* issued, the Supreme Court confirmed the critical public notice function of Section 112, Paragraph 2. *See Nautilus, Inc. v. Biosig Instruments, Inc*., 134 S. Ct. 2120, 2130 (2014) (warning against "diminish[ing] the definiteness requirement's public-notice function" and "foster[ing] the innovation-discouraging zone of uncertainty against which this Court has warned") (citation and internal quotation marks omitted).

Claim 13 of the '882 patent, and claim 19 of the '473 patent are all indefinite under *IPXL*. Claim 13 of the '882 patent is directed to a "system that allocates shared memory" comprising "a transceiver." The claim then recites that the transceiver "performs" a list of method steps: "transmitting or receiving a message…," "determining an amount of memory…," "allocating a first number of bytes…," "allocating a second number of bytes…," and "deinterleaving the first plurality of RS coded data bytes… ." The use of the present participle ("ing") within the claim indicates the presence of method steps. *Compare Sound View Innovations*, 2017 WL 2221177, at *9 (observing that claim language using "the present participle form of verbs" such as

"receiving" and "repeating" is "suggestive of method claiming" and finding claim indefinite under *IPXL*). The system claim's ordered references to transmitting or receiving a message, allocating a first number of bytes, and allocating a second number of bytes likewise bears the hallmarks of method claiming. *See id*. at *10 (finding that recitation of a "first" message received and a "second" message received indicated "order," as one aspect of method claiming). The first step of the claim recites an apparatus, which would normally indicate that merely buying, using, or selling the apparatus would infringe the claim. The later limitations introduce method steps, such as receiving messages and allocating memory. Viewed by themselves, these would be method steps that would have to be performed in order for the claim to be infringed. Viewed together, it is unclear whether a system with a transceiver itself infringes, or whether the transceiver must be used to perform each of the recited steps to infringe. Thus, this claim is indefinite. *Sound View Innovations*, 2017 WL 2221177, at *8; *IPXL*¸ 430 F.3d at 1384.

Claim 19 of the '473 patent is also indefinite because it is unclear when infringement might occur. Claim 19 recites an apparatus, "a multicarrier communications transceiver," but later steps recite "wherein the memory is allocated between" interleaving and deinterleaving functions in accordance with a message "received during initialization of the transceiver." The claim recites an apparatus, but also indicates that the invention requires allocating memory in accordance with a message received during initialization. This implies that the message must have been received, and the memory must have been allocated according to the message to practice the invention. One of ordinary skill in the art would not know whether infringement occurred merely by owning the transceiver, or if the memory must be allocated in advance, or already allocated when sold, to infringe. Thus, this claim is indefinite. *Sound View Innovations*, 2017 WL 2221177, at *8; *IPXL*¸ 430 F.3d at 1384. 2Wire incorporates by reference Defendants'

portions of the Parties' Joint Claim Construction Brief for Family 3 Patents, and any declarations in support, regarding these terms and invalidity under *IPXL* as if fully set forth herein.

V. INVALIDITY CONTENTIONS FOR PATENT FAMILY 4

A. Invalidity Under 35 U.S.C. § 101

2Wire contends that the Asserted Family 4 Claims are invalid for failing to recite patentable subject matter under 35 U.S.C. § 101. In particular, claim 26 of the '627 Patent, claim 14 of the '041 Patent, and claim 14 of the '008 Patent are invalid for claiming no more than an abstract idea or principle. In *Alice Corp. Pty. v. CLS Bank Int'l*, 134 S. Ct. 2347 (2014), the Supreme Court set forth a two-part test for determining whether a claim recites patent-eligible subject matter. First, the court must determine whether the claims at issue are directed toward laws of nature, natural phenomena, or abstract ideas. *Id.* at 2355. Second, if the claims are directed toward ineligible subject matter, the court must then consider the claim elements – both individually and as an ordered combination – to determine whether they add an "inventive concept." *Id.* Merely claiming a generic "computer" to implement an abstract idea is not sufficient to transform the computer into a patent-eligible invention. *Id.* at 2357-50.

Here, claim 26 of the '627 Patent, claim 14 of the '041 Patent, and claim 14 of the '008 Patent are drawn to no more than the abstract idea of scrambling the phases of input bit streams in a multicarrier system to reduce the incidence of signal clipping and transmission errors. Multicarrier systems themselves were known in the art long before the earliest effective filing date of the Family 4 Claims. Signal clipping is a long-standing, well-known issue in multicarrier systems, and phase scrambling is a well-known engineering practice. *See, e.g.*, U.S. Patent No. 2,229,387 (patent issued in 1942 stating that "The use of synchronizing impulses for correcting the phase relation of rotary apparatus at a receiving station is well-known and highly developed in the fields of automatic telegraphy and television."). The phase scrambling recited by claim 26

of the ’627 Patent, claim 14 of the ’041 Patent, and claim 14 of the ’008 Patent are mere well-understood, routine and conventional mathematical transformations. Nor are these claims tethered to a particular implementation or environment with respect to phase scrambling and calculating a phase shift. For example, the recitation of a “transceiver” does not impart structure to the claims as the specification teaches that the phase shifting can be executed by software. *See, e.g.*, ’627 Patent, col. 4:43-51; *see also* ’041 Patent, col. 4:38-46. Moreover, claim 26 of the ’627 Patent, claim 14 of the ’041 Patent, and claim 14 of the ’008 Patent are not tied to, and do not recite, any specific algorithm, nor do they disclose any special-purpose processor.

B. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

Claim 26 of the ’627 Patent, claim 14 of the ’041 Patent, and claim 14 of the ’008 Patent are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 6,625,219 (“Stopler”)
- U.S. Patent No. 6,963,599 (“Dunn”)
- U.S. Patent No. 6,125,103 (“Bauml”)
- U.S. Patent No. 5,682,376 (“Hayashino”)
- U.S. Patent No. 6,556,557 (“Cimini”)
- U.S. Patent No. 5,903,614 (“Suzuki ’614”)
- U.S. Patent No. 6,301,268 (“Laroia”)
- U.S. Patent No. 6,781,951 (“Fifield”)
- U.S. Patent No. 6,310,869 (“Holtzman”)
- U.S. Prov. App. Ser. No. 60/164,134 (applicant’s admissions)
- U.S. Patent No. 7,292,627 (“Tzannes ’627”)
- U.S. Patent No. 7,471,721 (“Tzannes ’721”)
- U.S. Patent No. 8,073,041 (“Tzannes ’041”)

- U.S. Patent No. 8,090,008 (“Tzannes ’008”)
- U.S. Patent No. 8,218,610 (“Tzannes ’610”)
- U.S. Patent No. 8,355,427 (“Tzannes ’427”)
- EP 0 743 768 A1 (“Narahashi”)
- U.S. Patent No. 6,088,406 (“Suzuki ’406”)
- EP 0 895 389 A2 Williams (“Williams”)
- U.S. Patent No. 4,924,516 (“Bremer”)
- U.S. Patent No. 6,657,949 (“Jones”)
- U.S. Patent No. 5,694,415 (“Suzuki ’415”)
- Boyd, IEEE Transactions on Circuits and Systems, Vol. Cas-33, No. 10, Oct. 1986 (“Boyd”)
- EP 0 552 034 A2 (“Kaku”)
- U.S. Patent No. 6,144,696 (“Shively”)
- U.S. Patent No. 6,590,893 (“Hwang”)
- U.S. Patent No. 6,590,860 (“Sakoda”)
- T1E1.4 Contribution No. T1E1.4/97-270 by Djokovic (“Djokovic”)
- T1.413-1995 – “Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface” (“T1.413-1995”)
- T1.413-Issue 2 – “Standards Project for Interfaces Relating to Carrier to Customer Connection of Asymmetrical Digital Subscriber Line (ADSL) Equipment,” June 5, 1998. (“T1.413 – 1998”)

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits G-1 through G-19, H-1 through H-19, and J-1 through J-19 demonstrate how the asserted claims of the ’627 Patent, ’041 Patent, and ’008 Patent are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the ’627 Patent, ’041 Patent, and ’008

Patent and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire reserves the right to assert that any claim element is disclosed in other portions of the cited references. In addition, 2Wire identifies, and incorporates herein by reference, all prior art of record in the prosecution history of the ’627 Patent, ’041 Patent, and ’008 Patent (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports, or specifications), any of which may anticipate and/or render the asserted claims obvious. Further, 2Wire identifies any TQ Delta patents that claim the same priority date as the ’627 Patent, the ’041 Patent, and the ’008 Patent and disclose the same subject matter and for which a terminal disclaimer was not filed during prosecution, under the doctrine of obviousness-type double patenting. This includes, but is not limited to, U.S. Patent No. 7,471,721 and U.S. Patent No. 8,218,610. Additional evidence regarding the features and elements of prior art references may be provided by witness testimony, or by additional documents and materials describing the prior art, that may be identified through the course of ongoing discovery and investigation.

To the extent that a reference above is found to be missing a limitation of the representative claims, any one of the prior art references identified above may be combined with one another or with any one or more of the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render the representative claims obvious under 35 U.S.C. § 103:

- U.S. Patent No. 5,694,415 (“Suzuki ’415”)

- U.S. Patent No. 5,896,419 ("Suzuki '419")
- U.S. Patent No. 6,233,247 ("Alami")
- U.S. Patent No. 6,240,141 ("Long")
- U.S. Patent No. 6,757,299 ("Verma")
- U.S. Patent No. 6,590,860 ("Sakoda")
- U.S. Patent No. 6,507,585 ("Dobson")
- U.S. Patent No. 4,408,298 ("Ruhland")
- U.S. Patent No. 3,811,038 ("Reddaway")
- U.S. Patent No. 4,672,629 ("Beier")
- U.S. Patent No. 4,924,516 ("Bremer")
- U.S. Patent No. 5,694,389 ("Seki")
- U.S. Patent No. 6,324,171 ("Lee")
- U.S. Patent No. 6,438,186 ("Strait")
- U.S. Patent No. 5,101,417 ("Richley")
- U.S. Patent No. 6,389,080 ("Barnes")
- U.S. Patent No. 6,081,502 ("Paneth")
- U.S. Patent No. 6,112,094 ("Dent")
- U.S. Patent No. 6,731,594 ("Bohnke")
- U.S. Patent No. 5,367,516 ("Miller")
- U.S. Patent No. 6,625,219 ("Stopler")
- U.S. Patent No. 6,963,599 ("Dunn")
- U.S. Patent No. 6,125,103 ("Bauml")
- U.S. Patent No. 5,682,376 ("Hayashino")
- U.S. Patent No. 6,556,557 ("Cimini")

- U.S. Patent No. 5,903,614 (“Suzuki ’614”)
- U.S. Patent No. 6,301,268 (“Laroia”)
- U.S. Patent No. 6,781,951 (“Fifield”)
- U.S. Patent No. 6,310,869 (“Holtzman”)
- EP 0 552 034 A2 (“Kaku”)
- EP 0 743 768 A1 (“Narahashi”)
- EP 0 895 389 A2 Williams (“Williams”)
- U.S. Patent No. 6,088,406 (“Suzuki ’406”)
- U.S. Patent No. 6,657,949 (“Jones”)
- M.J.E. Golay, “Complementary Series,” IRE Trans. on Information Theory, Apr. 1961 (“Golay”)
- S. Narahashi and T. Nojima, “A New Phasing Scheme for Multitone Signal Systems to Reduce Peak-to-Average Power Ratio,” Elecs. and Commn’s in Japan, Part 1, Vol. 80, No. 1.
- Mestdagh, D.J.G and P.M.P. Spruyt, “A Method to Reduce the Probability of Clipping in DMT-Based Transceivers,” IEEE Trans. on Communications, Vol. 44, No. 10.
- Bauml, R.W. et al., “Reducing the Peak-to-Average Power Ratio of Multicarrier Modulation by Selected Mapping,” Electronics Letters, Vol. 32, No. 22.
- Muller, S.H. and J.B. Huber, “A Novel Peak Power Reduction Scheme for OFDM,” IEEE 1997.
- T1.413-Issue 2 – “Standards Project for Interfaces Relating to Carrier to Customer Connection of Asymmetrical Digital Subscriber Line (ADSL) Equipment,” June 5, 1998. (“T1.413 – 1998”)
- ANSI Technical Report, TR-004, Network Migration (“TR-004”)
- T1E1.4 Contribution No. T1E1.4/97-270 by Djokovic (“Djokovic”)
- T1.413-1995 – “Network and Customer Installation Interfaces – Asymmetric Digital Subscriber Line (ADSL) Metallic Interface” (“T1.413-1995”)

Specific combinations that render TQ Delta’s Asserted Claims obvious under 35 U.S.C. § 103

using these references are set forth in Exhibits G-1 though G-19, H-1 through H-19, and J-1 through J-19. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the ’627 Patent, the ’041 Patent, and the ’008 Patent (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports or specifications), to render the asserted claims obvious. Further, any of the foregoing anticipatory or secondary prior art references listed above may be combined with one another to render the asserted claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or more of the prior art references identified above to arrive at the combination of elements recited in each asserted claim. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable

expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results.

By way of example only, the Patent Trial and Appeal Board has concluded that it would have been obvious for one of skill in the art to combine Stopler and Shively because the combination is the use of a known technique to improve a similar device, method or product in the same way. IPR2016-01021, Paper 44 at 18, 28-35. Similar reasoning applies to any combination of multicarrier communication devices and references teaching phase adjustment or randomization and scrambling techniques. One of skill in the art would have known that multicarrier transmission techniques suffer from the disadvantage of high peak power during transmission from constructive overlap of the subchannels. *See, e.g.*, Bauml at Abstract, 1:46-50; Jones at 5:49-56; T1.413-1998 at p.40. This is particularly true when multiple subchannels carry the same information. The applicant admitted that sending the same data bits on different carriers was a well-known method to decrease bit error rate and further admitted that sending the same data bits on multiple carriers was a known cause of the known problem of high peak-to-average power ratio in a transmission signal. U.S. Prov. App. Ser. No. 60/164,134 at 1-2. One of skill in the art would have also known that adjusting the phase characteristics of carrier signals in order to scramble the transmission signal was a known method to address high peak-to-average

ratio in a transmission signal. For example, Boyd, IEEE Transactions on Circuits and Systems, Vol. Cas-33, No. 10, Oct. 1986, at 1019, explains that the crest factor, or peak to average ratio, of a multitone signal is improved by the use of a random pattern of phases. As a further example, Jones explains that phase scrambling can be used when certain combinations of data symbols will result in an excessive peak to average power ratio. Jones at 5:44-56. As a further example, Williams explains that randomization of constellation points using a pseudo-random number sequence (that can be replicated to de-randomize on the receiver side) can be used to prevent undesirable large impulses in a transmission signal that would cause distortion close to the saturation or clipping point. Williams at ¶ 44. The foregoing citations are illustrative only. The prior art, including the prior art references detailed in Exhibits G-1 through G-19, H-1 through H-19, and J-1 through J-19 contain ample additional disclosures establishing these points.

When designing a multicarrier system, particularly one in which the same data bits are or may be sent on multiple carriers, one of skill in the art would have known of the peak-to-average ratio issue and looked to other references in the telecommunications field describing how to adjust the phases of the carriers in order to scramble the transmission signal and address the peak-to-average ratio issue. To the extent that any references teaching adjusting the phases of carriers are not explicitly multicarrier systems, one of skill in the art would have understood that the teaching could be applied to each carrier in a multicarrier system in order to adjust the phases of the carriers relative to each other. Combining various references describing how to adjust the phases of the carriers in order to scramble the transmission signal with references teaching a multicarrier communication system in order to address the peak-to-average ratio issue is nothing more than using a known technique to improve a similar device, method, or product in the same

way. Moreover, market forces would have motivated one of skill in the art to make these combinations. As admitted by the applicant, it was known in the art that high peak-to-average ratio can adversely affect power consumption and component requirements. ’627 patent col. at 2:5-9. In addition, it was known in the art and admitted as known by the applicant that high peak-to-average power ratio can cause signal clipping, which results in transmission errors. *See, e.g.*, T1.413-1998 at p. 40; U.S. Prov. App. Ser. No. 60/164,134 at 1. One of skill in the art would have been well aware of these adverse effects. A skilled artisan would have looked for ways to address the peak-to-average power ratio issue to mitigate those adverse effects and would have known that phase scrambling of the carriers provided a known solution.

The motivation to combine references and specific illustrative references used above are exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire’s invalidity charts and expert report(s) on invalidity.

2Wire reserves the right to amend and supplement these § 102 contentions as further information and discovery are obtained including, in particular, with regard to the alleged conception and reduction-to-practice of the patents-in-suit.

C. Invalidity Under 35 U.S.C. § 112

2Wire lists below exemplary grounds upon which the asserted claims are invalid for failure to meet one or more requirements of 35 U.S.C. ¶ 112. A more detailed basis for 2Wire’s written description, enablement, and indefiniteness defenses will be set forth in 2Wire’s expert report(s) on invalidity. Furthermore, 2Wire has not yet had an opportunity to conduct full discovery regarding invalidity (e.g., inventor depositions, etc.). 2Wire has therefore been unable

to fully evaluate and formulate these and other invalidity contentions. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112. Such supplementation and/or amendments may include, but are not limited to, invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement should the claims be construed under 35 U.S.C. § 112 ¶ 6.

Invalidity Under 35 U.S.C. § 112 ¶ 1: The asserted claims are invalid because the patent specification does not include sufficient description of the subject matter claimed, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the claimed subject matter without undue experimentation. In addition, the specification to which TQ Delta apparently seeks priority does not describe the full scope of each asserted claim with particularity, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "a multicarrier modulation transceiver [a multicarrier system including a first transceiver] that uses [a transmission signal having] a plurality of carrier signals for modulating an input bit stream" ('627 Patent, claim 26; '008 Patent, claim 14)
- "wherein the multicarrier modulation transceiver is capable of associating each carrier signal with a value determined independently of any input bit value" ('627 Patent, claim 26)
- "computing a phase shift for each carrier signal based on the value associated with that carrier signal" ('627 Patent, claim 26)

- “combining the phase shift computed for each carrier signal with the phase characteristic of that carrier signal so as to substantially scramble the phase characteristics of the plurality of carrier signals” (’627 Patent, claim 26)
- “wherein the value varies with each DMT symbol” (’627 Patent, claim 26)
- “a phase shift for each carrier signal is based on . . . the combining of a phase shift for each carrier signal with the phase characteristic of that respective carrier signal so as to substantially scramble the phase characteristics of the plurality of carrier signals” (’041 Patent, claim 14)
- “multiple carrier signals corresponding to the plurality of phase shifted and scrambled carrier signals are used by the first multicarrier transceiver to demodulate a same input bit value of the received bit stream” (’041 Patent, claim 14)
- “combining the phase shift computed for each respective carrier signal with the phase characteristic of that carrier signal to substantially scramble the phase characteristics of the plurality of carrier signals” (’008 Patent, claim 14)
- “wherein multiple carrier signals corresponding to the scrambled carrier signals are used by the first transceiver to modulate the same bit value” (’008 Patent, claim 14).

The asserted claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

2Wire’s accused products do not infringe the representative claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire. To the extent that TQ

Delta contends that the asserted claims have been construed so broadly as to cover the accused products, such a construction would render the asserted claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: The asserted claims are also invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed. 2Wire contends that a person of ordinary skill in the art to which the claimed subject matter pertains would not understand the scope of each asserted claim when read in light of the specification. By way of example, and without limitation, at least the following claim terms are indefinite under Section 112:

- "substantially scramble the phase characteristics of the plurality of carrier signals" ('627 Patent, claim 26; '041 Patent, claim 14; '008 Patent, claim 14)
- "multiple carrier signals corresponding to the plurality of phase shifted and scrambled carrier signals are used by the first multicarrier transceiver to demodulate a same input bit value of the received bit stream" ('041 Patent, claim 14)
- "multiple carrier signals corresponding to the scrambled carrier signals are used by a the first multicarrier transceiver to modulate the same bit value" ('008 Patent, claim 14)
- "wherein the value varies with each DMT symbol" ('627 Patent, claim 26)
- "A multicarrier modulation transceiver that uses a transmission signal having a plurality of carrier signals for modulating an input bit stream" ('627 Patent, claim 26)
- "wherein the multicarrier modulation transceiver is capable of associating each

carrier signal with a value determined independently of any input bit value" ('627 Patent, claim 26)

- "transceiver" ('627 Patent, claim 26; '041 Patent, claim 14)
- "a first transceiver that uses a plurality of carrier signals for receiving a bit stream" ('041 Patent, claim 14)
- "the transceiver capable of receiving a bit stream" ('041 Patent, claim 14)
- "a phase shift for each carrier signal is based on . . . the combining of a phase shift for each carrier signal with the phase characteristic of that respective carrier signal" ('041 Patent, claim 14)

The asserted claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regard as their invention.

Further, the representative claims are invalid under Section 112 because they purport to claim both an apparatus and a method of using the apparatus. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005).

2Wire reserves the right to supplement and/or amend its contentions.

VI. INVALIDITY CONTENTIONS FOR PATENT FAMILY 5

The Court has not yet entered a Claim Construction Order for the Family 5 patents, which may include decisions on the invalidity of the Asserted Family 5 Claims. 2Wire reserves the right to amend its invalidity contentions in response to the Court's Family 5 Claim Construction Order, once it is entered.

A. Invalidity Under 35 U.S.C. § 101

Claims 11 and 16 of the '379 Patent and claims 10 and 16 of the '337 Patent are invalid

for failing to recite patentable subject matter under 35 U.S.C. § 101. Section 101 provides that "[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title." Mathematical equations generally are not patentable subject matter under § 101. *See, e.g., Bilski v. Kappos*, 561 U.S. 593, 612 (2010) ("The concept of hedging, described in claim 1 and reduced to a mathematical formula in claim 4, is an unpatentable abstract idea, just like the algorithms at issue in *Benson* and *Flook*. Allowing petitioners to patent risk hedging would pre-empt use of this approach in all fields, and would effectively grant a monopoly over an abstract idea").

Here, TQ Delta concedes that the asserted claims of the Family 5 patents cover nothing more than a mathematical equation. *See* Transcript of *Markman* Hearing, January 10, 2018 at *e.g.*, 51:20-52:2 (Court asks whether the specification "just giv[es] a couple of these equations and that's all you do, is what it thinks normalizing is?" and TQ Delta's counsel responds: "Correct."). Claims 11 and 16 of the '379 Patent are drawn to no more than the abstract idea of identifying CRC errors and normalizing a count of those CRC errors. "CRC" stands for "cyclic redundancy checksum" and was a well-known method of checking for errors in data transmission long before the alleged invention of the Family 5 Patents. Detection of CRC errors, determining a local CRC octet, comparing a local CRC octet to a received octet, and identifying when the local CRC is not identical to the received octet are long-standing, well-known engineering practices. The normalization of errors and error reporting is a long-standing, well-known mathematical practice. Claim 16 simply specifies a mathematical equation (PERp/K), for doing so. Neither claim 11 nor claim 16 requires that the claimed "module" do anything with the normalized error count. For example, the asserted claims do not require reporting the normalized

error count, nor do they require taking any action based on the normalized error count. Moreover, claims 11 and 16 are untethered to any specific implementation or environment because the patentee did not limit the claimed "Cyclic Redundancy Checksum (CRC) anomaly counter normalization module," "CRC bit computation module," "CRC bit comparison module," or "CRC error reporting module" in any way. The patent itself states that these elements can be implemented in hardware, software, or any combination of the two. *See, e.g.*, '379 Patent, col. 9:49-10:27.

Claims 10 and 16 of the '337 Patent are likewise drawn to no more than the abstract idea of normalizing a CRC anomaly counter and reporting when a certain number of anomalies is reached in a certain period of time. Detecting and counting CRC errors, and normalizing them based on a computation period were long-standing, well-known mathematical and engineering practices. Claim 16 merely specifies a mathematical equation (PERp/K). Neither claim 10 nor claim 16 requires that the claimed "transceiver" do anything with the normalized error count. For example, the asserted claims do not require reporting the normalized error count, nor do they require taking any action based on the normalized error count. Claims 10 and 16 of the '337 Patent are also untethered to any specific implementation or environment, and neither the claims, nor the specification place limits on the structure or function of a "transceiver," or of a "CRC anomaly counter" in any way.

In addition, claims 11 and 16 of the '379 Patent and claims 10 and 16 of the '337 Patent risk preempting all ways of calculating, reporting, and normalizing CRC errors.

B. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

2Wire contends that claim 16 of the '379 Patent and/or claims 10 and 16 of the '337 Patent are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 6,094,465 ("Stein")

- U.S. Patent No. 6,598,189 ("Zhao")
- U.S. Patent No. 7,010,001 ("Odenwalder")
- U.S. Patent No. 7,487,430 ("Kim")
- Seyhan Civanlar & Bharat T. Doshi, "Self-Healing in Wideband Packet Networks," IEEE Network Magazine, January 1990 ("Civanlar")
- U.S. Patent App. Pub. No. 2003/0185212 ("Kelly")
- ITU-T Recommendation G.997.1, "Physical Layer Management for Digital Subscriber Line (DSL) Transceivers" ("G.997.1")
- ITU-T Recommendation G.997.1 (06/1999), "Physical Layer Management for Digital Subscriber Line (DSL) Transceivers" ("G.997.1-1999")
- ITU-T Recommendation G.992.3 (07/2002) "Asymmetric digital subscriber line transceivers 2 (ADSL2)" ("G.992.3-2002")
- ITU-T SG 15/Q4 Contribution, COM 15-D1185-E, "VDSL2: Proposal on VDSL2 Framing" by Thyagarajan Umashankar ("D1185")
- "Network Management Standards: Approaches by T1M1 and the LEC Perspective" by R. Pyle ("Pyle")
- IEEE T1E1.4 Working Group Document T1E1.4/98-024, "Liaison regarding performance monitoring requirements for DSL," January 15, 1998
- IEEE T1E1 Working Group Document T1E1.4/98-180, "Liaison to T1E1.4 on ADSL Performance Parameters," May 22, 1998

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits K-1 through K-9 and L-1 through L-6 demonstrate how TQ Delta's Asserted Claims of the '379 Patent and '337 Patent are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the '379 Patent and '337 Patent and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire

reserves the right to assert that any claim element is disclosed in other portions of the cited references. In addition, 2Wire identifies, and incorporates here by reference, all prior art of record in the prosecution history of the ’379 Patent and ’337 Patent (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports, or specifications), any of which may anticipate and/or render TQ Delta’s Asserted Family 5 Claims obvious. Further, 2Wire identifies any TQ Delta patents that claim the same priority date as the ’379 Patent and the ’337 Patent and disclose the same subject matter and for which a terminal disclaimer was not filed during prosecution, under the doctrine of obviousness-type double patenting. This includes, but is not limited to, U.S. Patent No. 7,979,778. Additional evidence regarding the features and elements of prior art references may be provided by witness testimony, or by additional documents and materials describing the prior art, that may be identified through the course of ongoing discovery and investigation.

To the extent that a reference above is found to be missing a limitation of TQ Delta’s Asserted Family 5 Claims, any one of the prior art references identified above may be combined with any one or more of the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render the claims obvious under 35 U.S.C. § 103:

- U.S. Patent No. 7,979,778 (“Tzannes”)
- U.S. Patent No. 5,936,972 (“Meidan”)
- U.S. Patent No. 6,934,885 (“Gabele”)
- U.S. Patent No. 5,220,567 (“Dooley”)
- U.S. Patent No. 7,032,157 (“Kim ’157”)
- U.S. Patent No. 7,206, 291 (“Soldani”)

- U.S. Patent No. 5,671,255 (“Wang”)
- U.S. Patent No. 5,613,061 (“Taylor”)
- U.S. Patent No. 6,546,509 (“Starr”)
- U.S. Patent No. 5,566,206 (“Butler”)
- U.S. Patent No. 5,751,725 (“Chen”)
- U.S. Patent No. 6,088,337 (“Eastmond”)
- U.S. Patent No. 6,128,763 (“LoGalbo”)
- U.S. Patent No. 6,734,810 (“Kajita”)
- U.S. Patent No. 7,302,379 (“Cioffi”)
- U.S. Patent No. 6,820,232 (“Kim”)
- U.S. Patent No. 6,519,738 (“Derby”)
- U.S. Patent No. 6,065,149 (“Yamanaka”)
- U.S. Patent No. 7,103,822 (“Glaise”)
- U.S. Patent No. 6,175,590 (“Stein”)
- U.S. Patent No. 6,094,465 (“Stein”)
- U.S. Patent No. 6,598,189 (“Zhao”)
- U.S. Patent No. 7,010,001 (“Odenwalder”)
- U.S. Patent No. 7,487,430 (“Kim”)
- U.S. Patent No. 7,451,379 (“Tzannes ’379”)
- U.S. Patent No. 7,925,958 (“Tzannes ’958”)
- U.S. Patent No. 7,979,778 (“Tzannes ’778”)
- U.S. Patent No. 8,516,337 (“Tzannes ’337”)
- U.S. Patent App. Pub. No. 2006/0228113 (“Cutillo”)
- U.S. Patent App. Pub. No. 2004/0198294 (“Hagin-Metzer”)

- U.S. Patent App. Pub. No. 2006/0245366 ("Binde")
- Seyhan Civanlar & Bharat T. Doshi, "Self-Healing in Wideband Packet Networks," IEEE Network Magazine, January 1990 ("Civanlar")
- U.S. Patent App. Pub. No. 2003/0185212 ("Kelly")
- ITU-T Recommendation G.997.1, "Physical Layer Management for Digital Subscriber Line (DSL) Transceivers" ("G.997.1")
- ITU-T SG 15/Q4 Contribution, COM 15-D1185-E, "VDSL2: Proposal on VDSL2 Framing" by Thyagarajan Umashankar ("D1185")
- "Network Management Standards: Aproaches by T1M1 and the LEC Perspective" by R. Pyle ("Pyle")
- Peterson, W.W. and D.T. Brown, "Cyclic Codes for Error Detection," Proceedings of the IRE, January 1961 ("Peterson")
- Huffman, W. Cary and V. Pless, "Fundamentals of Error Correcting Codes," Cambridege University Press, 2003.
- Koopman, "32-Bit Cyclic Redundancy Codes for Internet Applications," The International Conference on Dependable Systems and Networks, 2002.
- Castagnoli et al., "Optimization of Cyclic Redundancy-Check Codes with 24 and 32 Parity Bits," IEEE Transactions on Communications, Vol. 41, No. 6, June 1993.
- Koopman, P. and T. Charkravarty, "Cyclic Redundanct Code (CRC) Polynomial Selection for Embedded Networks," The International Conference on Dependable Systems and Networks, 2004.
- IETF Network Working Group, Request for Comment 3276, "Definitions of Managed Objects for High Bit-Rate DSL – 2nd Generation (HDSL2) and Single-Pair High-Speed Digital Subscriber Line (SHDSL) Lines," May 2002
- ITU-T Recommendation G.826 entitled "End-to-End Error Performance Parameters and Objectives for International, Constant Bit-Rate Digital Paths and Connections" ("G.826")
- ITU SG 15 – Temporary Document SI-064 – Aware, Inc. – "ADSL: CRC Counter Normalization Procedure for SRA and DRR" ("SI-064")
- ITU SG 15 – Temporary Document LBU19R1 – Editor of recommendation G.997.1 – "G.ploam.bis Issues List ("LB-U19R1")

- IEEE T1E1.4 Working Group Document T1E1.4/98-024, "Liaison regarding performance monitoring requirements for DSL," January 15, 1998
- IEEE T1E1 Working Group Document T1E1.4/98-180, "Liaison to T1E1.4 on ADSL Performance Parameters," May 22, 1998
- Applicants' admitted prior art as described in the specification and related application

Specific combinations that render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103 using these references are set forth in Exhibits K-1 through K-9 and L-1 through L-6. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the '379 Patent and '337 Patent (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports or specifications), to render TQ Delta's Asserted Family 5 Claims obvious. Further, any of the foregoing anticipatory or secondary prior art listed above may be combined with one another to render TQ Delta's Asserted Family 5 Claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or more of the prior art references identified above to arrive at the combination of elements recited in each of TQ Delta's Asserted Family 5 Claims. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field, high-speed telecommunications and DSL systems. In addition, it would have been obvious to try combining

the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. The combination of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable expectation of success. Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. For example, error correction and monitoring based on cyclic redundancy check codes were known long before the priority date of the Family 5 Asserted Patents, and were commonly in use in telecommunications, including DSL systems. In addition, the ability of DSL systems to carry data at different rates was long known to those of ordinary skill in the art. It would have been a simple step to adjust the manner and scale in which CRC errors are reported.

Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results. The motivation to combine references is exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire’s invalidity charts and expert report(s) on invalidity following claim construction

and discovery on validity issues.

There are no secondary considerations of non-obviousness pertinent to the obviousness of the subject matter of the asserted claims. To the extent that TQ Delta raises any secondary considerations of non-obviousness, for example, in its expert reports, 2Wire reserves the right to address any such considerations, including by taking discovery on those issues and supplementing and/or amending its invalidity contentions as well as through 2Wire's expert report(s).

In addition, the Asserted Family 5 Claims are invalid under the printed matter doctrine because certain limitations claim printed matter (i.e., content of information) that is not functionally or structurally related to the medium containing the printed matter. In the alternative, the Asserted Family 5 Claims are invalid under the printed matter doctrine because certain limitations claim printed matter and are not entitled to patentable weight, without which the claims are anticipated or rendered obvious by the cited references. By way of example and not of limitation, printed matter includes limitations directed to the value by which a CRC anomaly counter is incremented "of M, wherein the value of M is equal to PERp/K, and K is a positive integer," and "wherein K is equal to 20 or 15."

2Wire does not presently have any disclosures under 35 U.S.C. § 102(f). However, 2Wire reserves the right to amend and supplement these § 102(f) contentions as further information and discovery are obtained including, in particular, with regard to the alleged conception and reduction-to-practice of the patents-in-suit.

C. Invalidity Under 35 U.S.C. § 112

2Wire lists below grounds upon which TQ Delta's Asserted Family 5 Claims are invalid for failure to meet one or more requirements of 35 U.S.C. ¶ 112. A more detailed basis for 2Wire's written description, enablement, and indefiniteness defenses will be set forth in 2Wire's

expert report(s) on invalidity. Furthermore, discovery regarding invalidity (e.g., inventor depositions, etc.) is ongoing. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112. Such supplementation and/or amendments may include, but are not limited to, invalidity contentions based on a failure to disclose the best mode of practicing the alleged invention and/or invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement should the claims be construed under 35 U.S.C. § 112 ¶ 6.

Invalidity Under 35 U.S.C. § 112 ¶ 1: TQ Delta's Asserted Family 5 Claims are invalid because the patent specification lacks sufficient description of the subject matter claimed, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the claimed subject matter without undue experimentation. In addition, the full scope of each claim was not described with particularity in the specification to which priority is apparently sought, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "A Cyclic Redundancy Checksum (CRC) anomaly counter normalization module designed to normalize a CRC anomaly counter based on a value for a CRC computation period (PERp)" ('379 Patent, claims 11 and 16)
- "a CRC bit computation module designed to determine a local octet based on a received bit stream" ('379 Patent, claims 11 and 16)
- "a CRC bit comparison module designed to compare the local CRC octet to a

received CRC octet" ('379 Patent, claims 11 and 16)

- "a CRC error reporting module designed to identify a CRC anomaly when the local CRC octet is not identical to the received CRC octet" ('379 Patent, claims 11 and 16)
- "normalizing of the CRC anomaly counter" ('379 Patent, claims 11 and 16)
- "a transceiver operable to normalize a CRC anomaly counter" ('337 Patent, claims 10 and 16)
- "when there are more than N CRC anomalies in a period of time" ('337 Patent, claims 10 and 16)

TQ Delta's Asserted Family 5 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

2Wire's accused products do not infringe TQ Delta's Asserted Family 5 Claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire, and any supplements thereto. To the extent TQ Delta's Asserted Family 5 Claims may eventually be construed so broadly as to cover the accused products, such a construction would render TQ Delta's Asserted Family 5 Claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: TQ Delta's Asserted Family 5 Claims are also invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed. 2Wire contends that a person of ordinary skill in the art to which the purported invention pertains would not understand the scope of each asserted claim when read in light of the specification. By way of example, and without limitation, at least the

following claim terms are indefinite under Section 112:

- "A Cyclic Redundancy Checksum (CRC) anomaly counter normalization module designed to normalize a CRC anomaly counter based on a value for a CRC computation period (PERp)" ('379 Patent, claims 11 and 16)
- "a CRC bit computation module designed to determine a local octet based on a received bit stream" ('379 Patent, claims 11 and 16)
- "a CRC bit comparison module designed to compare the local CRC octet to a received CRC octet" ('379 Patent, claims 11 and 16)
- "a CRC error reporting module designed to identify a CRC anomaly when the local CRC octet is not identical to the received CRC octet" ('379 Patent, claims 11 and 16)
- "normalizing of the CRC anomaly counter" ('379 Patent, claims 11 and 16)
- "a transceiver operable to normalize a CRC anomaly counter" ('337 Patent, claims 10 and 16)
- "when there are more than N CRC anomalies in a period of time" ('337 Patent, claims 10 and 16)

TQ Delta's Asserted Family 5 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regard as their invention.

Further, TQ Delta's Asserted Family 5 Claims are invalid under Section 112 because they purport to claim both an apparatus and a method of using the apparatus. To the extent that TQ Delta's Asserted Family 5 Claims invoke 35 U.S.C. § 112, ¶ 6 (pre-AIA), those claims are

invalid for failing to recite sufficient structure to perform the recited function. *See Williamson v. Citrix Online, LLC*, 792 F.3d 1339 (Fed. Cir. Jun. 16, 2015) (en banc). For example, the specification does not recite corresponding structure for the "Cyclic Redundancy Checksum (CRC) anomaly counter normalization module," "CRC bit computation module," "CRC bit comparison module," or "CRC error reporting module" recited in claims 11 and 16 of the '379 Patent.

The Federal Circuit explained in *Williamson* that when determining whether a claim is subject to Section 112, ¶ 6, the "essential inquiry is not merely the presence or absence of the word 'means' but whether the words of the claim are understood by persons of ordinary skill in the art to have a sufficiently definite meaning as the name for structure." *Id*. at 1348. Section 112, ¶ 6 applies to a claim term that does not use the word "means" when "the claim term fails to 'recite sufficiently definite structure' or else recites 'function without reciting sufficient structure for performing that function.'" *Id*. at 1349 (citation omitted). The disclosure requirement applies even where a skilled artisan might be able to devise a structure to perform the claimed function. *See Blackboard, Inc. v. Desire2Learn, Inc*., 574 F.3d 1371, 1385 (Fed. Cir. 2009) ("A patentee cannot avoid providing specificity as to structure simply because someone of ordinary skill in the art would be able to devise a means to perform the claimed function."). A claim can meet the paragraph 1 enablement requirement of section 112 but still fail under paragraph 6. *See, e.g., Atmel Corp. v. Information Storage Devices, Inc*., 198 F. 3d 1374, 1382 (Fed. Cir. 1999) ("Section 112, ¶ 6, however, does not have the expansive purpose of ¶ 1. It sets forth a simple requirement, a quid pro quo, in order to utilize a generic means expression. All one needs to do in order to obtain the benefit of that claiming device is to recite some structure corresponding to the means in the specification, as the statute states, so that one can readily ascertain what the

claim means and comply with the particularity requirement of ¶ 2.") (emphasis added). But "[f]ulfillment of the § 112, ¶ 6 tradeoff cannot be satisfied when there is a total omission of structure. There must be structure in the specification." *Id*.

The Federal Circuit also recognized in *Williamson* that the term "module" is a "well-known nonce word that can operate as a substitute for 'means' in the context of § 112, para. 6." *Williamson*, 792 F.3d at 1350 ("It replaces the term 'means' with the term 'module' and recites three functions performed by the 'learning control module.'"). "[T]he term 'module' does not provide any indication of structure because it sets forth the same black box recitation of structure for providing the same specified function as if the term 'means' had been used." *Id*.

Here, each of the "module" terms are described in the claims as being "designed to" perform *functions* relating to determining, comparing, identifying, computing, and normalizing. Notably, the patentee specifically defined the term "module" even more broadly than the "generic description" that the Federal Circuit found invoked Section 112, ¶ 6 in *Williamson*: "The term module as used herein can refer to *any known or later developed hardware, software, firmware, or combination thereof that is capable of performing the functionality associated with that element*." '379 Patent at 4:19-22 (emphasis added). By that definition, the patentee expansively defined the term "module" as used in its claims expressly to be without any specific structure at all. That each "module" is part of a transceiver does not remedy this express disclaimer of any sufficiently definite structure in the specification, nor does the file history of the Family 5 patents fill in the gap. The "[adjective] module [performing a function]" grammatical structure tracks the classic "means for [performing a function]" language and renders the term subject to Section 112, ¶ 6. Moreover, none of the verbiage (e.g., "CRC bit computation") surrounding the "module" terms had common or generally understood meanings

at the time of the alleged invention. No corresponding structures are identified in the specification. Indeed, the figures depict black boxes covering any means for achieving the claimed functions. *See, e.g.*, ’379 patent at 3:27-28 (“FIG. 1 is a *functional block diagram* illustrating an exemplary communication system according to this invention”) (emphasis added). Moreover, to the extent that the claimed functions are accomplished merely using software, no specific algorithm is disclosed to perform the claimed function. Thus, claims 11 and 16 of the ’379 patent are subject to the requirements of 35 U.S.C. § 112, ¶ 6, and invalid for failure to satisfy those requirements. 2Wire hereby incorporates by reference Defendants’ sections of the Parties’ Joint Claim Construction Brief for Family 5 Patents (D.I. 374), and any declarations in support, as if fully set forth herein.

To the extent that claims 11 and 16 of the ’379 patent do not invoke 35 U.S.C. § 112, ¶ 6 (pre-AIA), those claims are invalid for merely claiming the function of an apparatus.

VII. INVALIDITY CONTENTIONS FOR PATENT FAMILY 6

A. Invalidity Under 35 U.S.C. § 101.

Claims 8 and 10 of the ’835 Patent are invalid for failing to recite patentable subject matter under 35 U.S.C. § 101. Section 101 provides that “[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.” Nonetheless, there are three recognized exceptions to Section 101: “laws of nature, physical phenomena, and abstract ideas.” *Bilski v. Kappos*, 561 U.S. 593, 601 (2010) (*quoting Diamond v. Chakrabarty*, 447 U.S. 303, 309 (1980)).

TQ Delta’s Asserted Family 6 Claims of the ’835 Patent are invalid for claiming no more than an abstract idea. In *Alice Corp. Pty. v. CLS Bank Int’l*, 134 S. Ct. 2347 (2014), the Supreme Court set out a two-part test for determining whether a claim recites patent-eligible subject

matter. First, the court must determine whether the claims at issue are directed toward laws of nature, natural phenomena, or abstract ideas. *Id.* at 2355. Second, if the claims are directed toward ineligible subject matter, the court must then consider the claim elements – both individually and as an ordered combination – to determine whether they add an "inventive concept." *Id.* Merely claiming a generic "computer" to implement an abstract idea is not sufficient to transform the computer into a patent-eligible invention. *Id.* at 2357-50.

Here, claims 8 and 10 of the '835 Patent are drawn to no more than the abstract idea of adjusting transmission settings from one value to another. Transmission using forward error correction and interleaver parameters is a long-standing, well-known engineering practice in the field of communication. The adjustment of the settings for those transmission techniques is similarly long standing and well-known. The claims are untethered to any specific implementation or environment. Nor do the elements of the claims – whether individually or as a whole – evidence any "inventive concept." Transmitting a signal using a forward error correction and interleaver setting and transmitting a flag signal were well-known as was the notion of changing the forward error correction and interleaver parameter setting on a codeword boundary. The claims recite only a conventional technological environment, such as a conventional transceiver, and conventional methods of communicating information, that were well-known at the time of the alleged invention. Moreover, the '835 Patent claims do not require the transceiver to do anything other than to send a signal in two settings and sending a flag signal to flag the switching of the setting. For example, the '835 Patent claims do not require processing the message, interpreting the information in the message, or taking any action based on the information in the message. Accordingly, claims 8 and 10 of the '835 Patent are invalid for failure to recite patentable subject matter.

B. Invalidity Under 35 U.S.C. § 102 and/or 35 U.S.C. § 103

2Wire contends that claims 8 and 10 of the ’835 Patent are anticipated and/or rendered obvious by at least the following references:

- U.S. Patent No. 5,699,365 (“Klayman”)
- U.S. Patent Application with Publication No. 2002/0080867 (“Abbas”)
- U.S. Patent No. 7,428,669 (“Cioffi”)
- ITU-T Recommendation G.992.3 (07/2002)
- U.S. Patent Application with Publication No. 2003/0174764 (“Mahany”)
- U.S. Patent No. 6,700,881 (“Kong”)
- ITU-T Recommendation G.992.1 (06/1999)
- ITU-T Study Group 15, Question 4 Contribution SC-060 (“SC-060”)

The patents, publications, and references identified above qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g). The charts identified as Exhibits M-1 through M-8 demonstrate how TQ Delta’s Asserted Family 6 Claims of the ’835 Patent are anticipated and/or rendered obvious by the references above. Each chart identifies certain prior art to the ’835 Patent and identifies at least one citation in the prior art reference where each claim element of the asserted claims is disclosed. Though the charts provide illustrative citations to where each claim element may be found in the prior art, the cited references may contain additional disclosures of each claim element as well, and 2Wire reserves the right assert that any claim element is disclosed in other portions of the cited references. In addition, 2Wire identifies, and incorporates here by reference, all prior art of record in the prosecution history of the ’835 Patent (and all related patents and applications), and all prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups’ publications, reports, or specifications), any of which may anticipate and/or render TQ Delta’s Asserted

Family 6 Claims obvious. Additional evidence regarding the features and elements of prior art references may be provided by witness testimony, or by additional documents and materials describing the prior art, that may be identified through the course of ongoing discovery and investigation.

To the extent that a reference above is found to be missing a limitation of TQ Delta's Asserted Family 6 Claims, any one of the prior art references identified above may be combined with any one or more of the following references, all of which qualify as prior art under 35 U.S.C. §§ 102(a), 102(b), 102(e), and/or 102(g), to render TQ Delta's Asserted Family 6 Claims obvious under 35 U.S.C. § 103:

- U.S. Patent No. 7,940,798 ("Puputti")
- U.S. Patent No. 6,182,264 ("Ott")
- U.S. Patent No. 7,706,287 ("Tanaka")
- U.S. Patent No. 7,343,543 ("Mantha")
- U.S. Patent No. 7,418,240 ("Hsu")
- U.S. Patent No. 7,372,901 ("Holcomb")
- U.S. Patent No. 7,257,764 ("Suzuki")
- U.S. Patent No. 7,197,067 ("Lusky")
- U.S. Patent No. 7,181,177 ("Pauli")
- U.S. Patent No. 7,170,432 ("Ettorre")
- U.S. Patent No. 7,024,596 ("Xin")
- U.S. Patent No. 6,983,414 ("Duschatko")
- U.S. Patent No. 6,982,964 ("Beering")
- U.S. Patent No. 6,928,603 ("Castagna")
- U.S. Patent No. 6,772,388 ("Cooper")

- U.S. Patent No. 6,732,323 (“Mitlin”)
- U.S. Patent No. 6,477,669 (“Agarwal”)
- U.S. Patent No. 6,266,348 (“Gross”)
- U.S. Patent No. 6,067,646 (“Starr”)
- U.S. Patent No. 5,907,563 (“Takeuchi”)
- U.S. Patent No. 5,828,677 (“Sayeed”)
- U.S. Patent No. 5,638,384 (“Hayashi”)
- U.S. Patent No. 5,546,411 (“Leitch”)
- U.S. Patent No. 5,436,917 (“Karasawa”)
- U.S. Patent No. 5,392,299 (“Rhines”)
- U.S. Patent No. 4,677,622 (“Okamoto”)
- U.S. Patent No. 4,644,544 (“Furaya”)
- U.S. Patent No. 4,541,091 (“Nishida”)
- U.S. Patent No. 4,716,567 (“Ito”)
- U.S. Patent No. 5,699,365 (“Klayman”)
- U.S. Patent Application with Publication No. 2002/0080867 (“Abbas”)
- U.S. Patent No. 7,428,669 (“Cioffi”)
- ITU-T Recommendation G.992.3 (07/2002)
- U.S. Patent Application with Publication No. 2003/0174764 (“Mahany”)
- U.S. Patent No. 6,700,881 (“Kong”)
- ITU-T Recommendation G.992.1 (06/1999)
- ITU-T Study Group 15, Question 4 Contribution SC-060 (“SC-060”)
- U.S. Patent Application with Publication No. 2007/0258487 (“Puputti”)
- U.S. Patent Application with Publication No. 2003/30193889 (“Jacobsen”)

- U.S. Patent Application with Publication No. 2002/0041570 ("Ptasinski")
- U.S. Patent Application with Publication No. 2001/0022810 ("Joo")
- EP0696108A1
- EP0923821B1
- "HomePlug 1.0 Powerline Communication LANs – Protocol Description and Performance Results version 5.4," International Journal of Communication Systems ("Lee")
- "Improving I/O Performance of Multimedia Servers," University of Oslo, Norway ("Halvorsen")
- "Turbo Coded OFDM System for Video Terrestrial Broadcasting," LTS3-ITS-STI EPFL Ecublens, 1015, Switzerland ("Lattuada")

Specific combinations that render TQ Delta's Asserted Claims obvious under 35 U.S.C. § 103 using these references are set forth in Exhibits M-1 through M-8. Defendant reserves the right to rely on the references listed above for motivation to combine, the state of the art and/or the background knowledge of one of ordinary skill in the art.

In addition, any of the foregoing anticipatory or secondary prior art references listed above may be combined with any of the prior art of record in the prosecution history of the '835 Patent (and all related patents and applications), or with any prior art ITU-T Recommendations or other industry publications (such as ATM Forum, Broadband Forum, or similar groups' publications, reports or specifications), to render TQ Delta's Asserted Family 6 Claims obvious. Further, any of the foregoing anticipatory or secondary prior art references listed above may be combined with one another to render TQ Delta's Asserted Family 6 Claims obvious.

Moreover, one of ordinary skill in the art would have been motivated to combine one or more of the prior art references identified above to arrive at the combination of elements recited in each of TQ Delta's Asserted Family 6 Claims. The suggestion or motivation to modify or combine references for obviousness purposes is provided by the explicit and implicit teachings

of the prior art identified by 2Wire, the knowledge of one of ordinary skill in the art, and/or the nature of the claimed invention and the problem(s) purportedly being solved. As an initial matter, 2Wire notes that each prior art reference is in or relates to the same field, high-speed data communications and DSL systems. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field or endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. For example, flag signals were known by those of ordinary skill in the art, and would have been one of a finite number of predictable ways to signal a change in transmission parameters in a DSL system during transmission. The combination of prior art references identified in these contentions would have been obvious because the combinations represent the known potential options with a reasonable expectation of success.

Additionally, one of ordinary skill in the art would have been motivated to create combinations identified in these contentions using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or teaching, suggestion, or motivation in the prior art generally. Also, market forces in the industry and the desire to improve features and performance would motivate the addition of features to systems as they become available, become smaller, become less expensive, become more commonly used, provide better performance, reduce costs, size or weight, or predictably achieve other clearly desirable results. One of ordinary skill in the art would have recognized that it would be desirable to be able to change transmission parameters during transmission in response to, for example, a change in data rate, without going through a modem retraining. Those in the industry, and those of

ordinary skill in the art would understand that such features may lead to more reliable, high-quality service for customers. The motivation to combine references is exemplary only, and should not be used to limit these disclosures. There would have been substantial motivation to combine the prior art references prior to the invention date, and 2Wire reserves the right to and intends to supplement the foregoing with expert and other testimony. More detailed bases for the motivation to combine specific references will be set forth in 2Wire's expert report(s) on invalidity.

To the extent that TQ Delta raises any secondary considerations of non-obviousness, for example, in its expert reports, 2Wire reserves the right to address any such considerations, including by taking discovery on those issues and supplementing and/or amending its invalidity contentions.

2Wire does not presently have any disclosures under 35 U.S.C. § 102(f). 2Wire reserves the right to amend and supplement these § 102(f) contentions as further information and discovery are obtained including, in particular, with regard to the alleged conception and reduction-to-practice of the patents-in-suit.

C. Invalidity Under 35 U.S.C. § 112

2Wire lists below grounds upon which TQ Delta's Asserted Family 6 Claims are invalid for failure to meet one or more requirements of 35 U.S.C. ¶ 112. A more detailed basis for 2Wire's written description, enablement, and indefiniteness defenses will be set forth in 2Wire's expert report(s) on invalidity. 2Wire reserves the right to supplement and/or amend these contentions based on Section 112. Such supplementation and/or amendments may include, but are not limited to, invalidity contentions based on indefiniteness, lack of written description, and/or lack of enablement.

<u>Invalidity Under 35 U.S.C. § 112 ¶ 1</u>: TQ Delta's Asserted Family 6 Claims are invalid

because the patent specification lacks sufficient description of the subject matter claimed, and the manner and process of using it, in such full, clear, concise, and exact terms as to enable any person of ordinary skill in the art to which it pertains to make and use the claimed subject matter without undue experimentation. In addition, the full scope of each claim was not described with particularity in the specification to which priority is apparently sought, thereby setting forth insufficient detail to allow one of ordinary skill in the art to understand what is claimed and to recognize that the inventor(s) invented what is claimed. By way of example, and without limitation, at least the following elements are not enabled and/or fail to meet the written description requirement of Section 112:

- "the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal" ('835 Patent, claims 8 and 10)
- "interleaver parameter value" ('835 Patent, claims 8 and 10)
- "FIP [setting/value]" ('835 Patent, claims 8 and 10)

TQ Delta's Asserted Family 6 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to meet the enablement and/or written description requirements of Section 112.

2Wire's accused products do not infringe TQ Delta's Asserted Family 6 Claims for at least the reasons set out in the non-infringement charts previously provided by 2Wire, 2Wire's interrogatory responses, and any supplements thereto. To the extent that TQ Delta's Asserted Family 6 Claims may eventually be construed so broadly as to cover the accused products, such a construction would render TQ Delta's Asserted Family 6 Claims invalid for failure to meet the requirements of Section 112, paragraph 1.

Invalidity Under 35 U.S.C. § 112 ¶ 2: TQ Delta's Asserted Family 6 Claims are also

invalid because they fail to particularly point out and distinctly claim the subject matter that the purported inventors claimed. 2Wire contends that a person of ordinary skill in the art to which the purported invention pertains would not understand the scope of each claim when read in light of the specification. By way of example, and without limitation, at least the following claim terms are indefinite under Section 112:

- "configurable to" ('835 Patent, claims 8 and 10)
- "pre-defined forward error correction boundary" ('835 Patent, claims 8 and 10)

TQ Delta's Asserted Family 6 Claims (and all other claims in the asserted patents that include or depend from any claims that include any of the above limitations) are invalid because they fail to particularly point out and distinctly claim the subject matter that the applicants regard as their invention. Moreover, TQ Delta repeatedly altered its position as to the potential meaning of "pre-defined forward error correction boundary," indicating that the scope and meaning of the limitation is indefinite.

Further, TQ Delta's Asserted Family 6 Claims are invalid under Section 112 because they purport to claim both an apparatus and a method of using the apparatus. *See IPXL Holdings, L.L.C. v. Amazon.com, Inc.*, 430 F.3d 1377 (Fed. Cir. 2005). For example, claim 8 of the '835 Patent recites an apparatus, then recites steps performed by the apparatus, such as "transmit signal using a first FIP setting," "transmit a flag signal," and "switch to using for transmission, a second FIP setting following transmission of the flag signal." Moreover, to the extent that the claimed functions are accomplished merely using software, no specific algorithm is disclosed to perform the claimed function. And to the extent that TQ Delta's Asserted Family 6 Claims do not invoke 35 U.S.C. § 112, ¶ 6 (pre-AIA), those claims are invalid for merely claiming the function of an apparatus. Thus, Asserted Family 6 Claim is invalid as indefinite under Section

112, paragraph 2.

August 15, 2018

By: /s/ Jody C. Barillare

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CERTIFICATE OF SERVICE

I, Jody C. Barillare, hereby certify that on August 15, 2018, a copy of DEFENDANT 2WIRE, INC.'S INVALIDITY CONTENTIONS IN RESPONSE TO TQ DELTA'S JULY 2, 2018 FINAL INFRINGEMENT CONTENTIONS was served on the following as indicated:

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/s/ Jody C. Barillare

EXHIBIT 9

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TQ DELTA, LLC, Plaintiff, v. 2WIRE, INC. Defendant.	Civil Action No. 13-cv-1835-RGA

OPENING EXPERT REPORT ON INVALIDITY OF DR. KRISTA S. JACOBSEN FOR FAMILY 3 PATENTS

Table of Contents

I. INTRODUCTION

1. My name is Krista S. Jacobsen. I have been asked by Defendant 2Wire, Inc. to provide this report in connection with the above-captioned District Court action. Specifically, I have been asked to opine on the validity of claim 1 of U.S. Patent No. 8,276,048 ("the '048 patent"), claim 5 of U.S. Patent No. 7,836,381 ("the '381 patent"), claim 13 of U.S. Patent No. 7,844,882 ("the '882 patent"), and claim 19 of U.S. Patent No. 8,495,473 ("the '473 patent"). I understand that plaintiff TQ Delta, LLC has alleged that certain 2Wire products infringe these claims. I further understand that these patents are referred to in this action as being part of "Family 3."

II. BACKGROUND AND QUALIFICATIONS

2. I was awarded a Ph.D. in Electrical Engineering from Stanford University in 1996, and a Master's Degree in Electrical Engineering in 1993, also from Stanford University. I held a National Science Foundation Graduate Fellowship from 1991-94 and an IBM Graduate Fellowship from 1994-95. In 1993, I was awarded an IEEE Communications Society Scholarship.

3. I hold a Bachelor of Science Degree in Electrical Engineering, summa cum laude, from the University of Denver, which I received in 1991. From 1986-91, I held a University of Denver Honors Scholarship, and from 1987-91, I held a Colorado Scholars Scholarship. I was elected to Phi Beta Kappa in 1988, and I received the University of Denver's Distinguished Senior Woman Award in 1990 and the University of Denver Pioneer Award in 1991. I won the Denver Section of the IEEE Student Paper Contest in 1991.

4. At Stanford, my Ph.D. research focused on technology for digital communications, including multicarrier modulation, discrete multi-tone (DMT) modulation, and orthogonal frequency division multiplexing (OFDM). My doctoral thesis topic was "Discrete

Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks." My research adviser was Dr. John M. Cioffi, who is known as the "father of digital subscriber lines (DSL)" and whose pioneering research in DSL earned him the Marconi Prize in 2006.

5. From 1996 to 2004, I worked as an engineer at Amati Communications Corporation, which was acquired by Texas Instruments (TI) in 1998. I was part of the team that developed the world's first operational DMT-based VDSL transceivers. From 2004 to 2006, as a consultant, I assisted clients to determine and execute DSL standardization and product strategies, wrote computer simulations of multicarrier systems, and generated and presented technical tutorials.

6. From 1996 through 2006, I participated in several standards-setting organizations that standardized DSL systems, including ATIS T1E1.4 (later renamed NIPP-NAI), ETSI TM6, ITU-T Study Group 15, Question 4, and IEEE 802.3ah (Ethernet in the First Mile). I wrote and/or presented many dozens of technical contributions to these organizations.

7. I am a co-editor of two books on DSL technology and the author of several book chapters on multicarrier modulation, DSL technology, and DSL standardization. In addition, I have authored or co-authored numerous technical papers and magazine articles on multicarrier communications, and, in 2001-02, I co-edited an issue of the IEEE Journal on Selected Areas in Communication focused on twisted pair transmission.

8. I have over ten years of experience working in the development and standardization of DSL technologies, including those embodied in the ITU-T Recommendations involved in the above-captioned District Court actions. I am an inventor named on eleven patents solving issues presented by or related to multicarrier modulation. My experience

includes work in DSL technologies and the DSL industry both before and after the purported priority date of the Family 2 patents.

9. I am also licensed to practice before the Patent and Trademark Office. I am currently an attorney who serves as an expert consultant and witness for patent litigation, and I provide patent prosecution and counseling services in multiple areas, including telecommunications.

10. A detailed curriculum vitae showing more of my credentials is attached to this report as Appendix A.

III. COMPENSATION

11. I am being compensated for my time at the rate of $400 per hour. This compensation is not contingent on my performance, the outcome of this matter, or any issues involved in or relating to this matter.

IV. DOCUMENTS AND OTHER MATERIALS RELIED UPON

12. In forming the opinions set forth in this declaration, I have reviewed each of the Family 3 patents that were asserted by TQ Delta in this action – U.S. Patent No. 7,831,890 ("the '890 Patent"), along with the '048, '381, '882, and '473 patents. Additionally, I have considered my own experience and expertise concerning the knowledge of a person having ordinary skill in the relevant art during the timeframe of the claimed priority date of the Family 3 patents. I have reviewed information generally available to, and relied upon by, a person having ordinary skill at the time of the alleged invention. I have also reviewed the parties' claim construction briefing and the Court's order on the same.

13. In addition, I have reviewed the materials listed in Appendix B.

14. I was told to assume that the earliest possible time of the alleged invention for each of the Family 3 patents is October 12, 2004, the date on which Provisional Application No.

60/618,269, was filed. I disagree, however, that the Family 3 patents are entitled to the priority date of the provisional application, as I explain below in Section VII.G.2. I am also informed, however, that once an accused infringer has introduced sufficient evidence to put at issue whether there is prior art alleged to anticipate the claims being asserted, and that prior art is dated earlier than the apparent effective date of the asserted patent claim, the patentee has the burden of going forward with evidence and argument to the contrary.

V. LEGAL PRINCIPLES

15. Although I am licensed to practice law, I am not offering any legal opinions in this Report. My opinions are based on the Court's constructions and, where the Court did not construe a term, the meaning that term would have had to a person having ordinary skill in the art in light of the specification and the prosecution history at the time of the filing of the earliest priority application.

A. Anticipation Under 35 U.S.C. § 102

16. I am informed and understand that to anticipate a patent claim under 35 U.S.C. § 102, a single asserted prior art reference must disclose each and every element of the claimed invention, either explicitly, implicitly, or inherently, to a person of ordinary skill in the art. There must be no difference between the claimed invention and the disclosure of the alleged prior art reference as viewed from the perspective of the person of ordinary skill in the art. Also, I understand that in order for a reference to be an anticipating reference, it must describe the claimed subject matter with sufficient clarity to establish that the subject matter existed and that its existence was recognized by persons of ordinary skill in the field of the invention. In addition, I am informed and understand that in order to establish that an element of a claim is "inherent" in the disclosure of an asserted prior art reference, extrinsic evidence (or the evidence outside the four corners of the asserted prior art reference) must make clear that the missing

element is necessarily found in the prior art, and that it would be recognized as necessarily present by persons of ordinary skill in the relevant field.

17. In my opinions below, when I say that a person of ordinary skill would understand, readily understand, or recognize that an element or aspect of a claim is disclosed by a reference, I mean that the element or aspect of the claim is disclosed explicitly to a person of ordinary skill in the art.

B. Obviousness Under 35 U.S.C. § 103

18. I am informed and understand that obviousness is a determination of law based on various underlying determinations of fact. In particular, these underlying factual determinations include (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time the claimed invention was made; (3) the differences between the claimed invention and the prior art; and (4) the extent of any proffered objective indicia of nonobviousness. I understand that the objective indicia that may be considered in such an analysis include commercial success of the patented invention (including evidence of industry recognition or awards), whether the invention fills a long-felt but unsolved need in the field, the failure of others to arrive at the invention, industry acquiescence and recognition, initial skepticism of others in the field, whether the inventors proceeded in a direction contrary to the accepted wisdom of those of ordinary skill in the art, and the taking of licenses under the patent by others, among other factors.

19. To ascertain the scope and content of the prior art, it is necessary to first examine the field of the inventor's endeavor and the particular problem for which the invention was made. The relevant prior art includes prior art in the field of the invention, and also prior art from other fields that a person of ordinary skill in the art would look to when attempting to solve the problem.

20. I understand that a claim may be rendered obvious if a person having ordinary skill in the art would understand the claimed invention as a predictable variation of a known reference.

21. I am informed and understand that an obviousness evaluation can be made using either a single reference or a combination of several prior art references. An obviousness analysis involving two or more references generally requires a reason why a person having ordinary skill in the relevant field would have combined aspects of those references in the way the asserted patent claims do. I understand that the prior art references themselves may provide a suggestion, motivation, or reason to combine, but other times the link may simply be common sense. An obviousness analysis can recognize that market demand, rather than scientific literature, often drives innovation, and that is sufficient motivation to combine references.

22. I understand that a particular combination of prior art references may be made by merely showing that it was obvious to try the combination. For example, common sense is a good reason for a person having ordinary skill to pursue known options when there is a design need or market pressure to solve a problem, and there are a finite number of identified, predictable solutions.

23. I am informed and understand that a determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. Instead, it is my understanding that in order to render a patent claim invalid as being obvious from a combination of references, there must be some evidence within the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination in a way that would produce the patented invention.

24. I am further informed and understand that a proper obviousness analysis focuses on what was known or obvious to a person having ordinary skill in the art, not just the patentee. Therefore, in an obviousness analysis, neither the motivation nor the purpose of the patentee is controlling. What is important is whether there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. For example, any need or known problem in the field at the time of the alleged invention that is supposedly addressed by the patent can provide a reason for combining the limitations in the manner claimed if a combination of prior art would address the same.

25. In addition, it is my understanding that in order to find a patent claim invalid for obviousness, there must be a finding that each element in each limitation of the patent claim is disclosed, taught, or suggested by the asserted combination of prior art references or elsewhere in the relevant prior art. I understand, however, that a patent claim composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. But multiple prior art references or elements may, in some circumstances, be combined to render a patent claim obvious. I understand that I should consider whether there is an "apparent reason" or motivation to combine the prior art references or elements in the way the patent claims. To determine whether such an "apparent reason" or motivation to combine the prior art references or elements in the way a patent claims exists, it will often be necessary to look to the interrelated teaching of multiple prior art references, to the effects of demands known to the design community or present in the marketplace, and to the background knowledge possessed by a person of ordinary skill in the art.

26. I am further informed and understand that when an element is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either

in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation of that available element, Section 103 likely renders the invention obvious. For the same reason, I am informed and understand that if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that such technique would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. Following these principles often requires one to look to interrelated teachings of multiple patents; the effects of demands known to the design community present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known element in the manner claimed by the patent at issue. I am further informed and understand that the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, because one can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

27. I am further informed and understand that although the use of the "teaching, suggestion or motivation" test for combining references has not been completely rejected, the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation, or by overemphasis on the importance of published articles and the explicit content of issued patents. I am informed and understand that in many fields there is little discussion of obvious techniques or combinations, and it is often the case that market demand, rather than scientific literature, drives design trends. Under the correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. Finally, I am informed and understand that common sense teaches that familiar items may have obvious

uses beyond their primary purposes and, in many cases, a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle.

28. I am also informed and understand that even though a prior art reference does not fully anticipate a claim of a patent, a claim may, nonetheless, be rendered obvious to one of ordinary skill in the art if the differences between the subject matter set forth in the patent claim and the prior art are such that the subject matter as a whole of the claim would have been obvious at the time the claimed invention was made.

29. I further am informed that in determining whether the claimed subject matter is obvious, one must also examine any objective indicia of nonobviousness (also called secondary considerations). I also have been informed that secondary considerations cannot overcome a strong showing of obviousness. In that regard, I am informed that secondary considerations must be commensurate in scope (proportional) with respect to the claims for which the evidence is offered to support. I have been informed that evidence of secondary considerations is not commensurate in scope if the claims are broader than the scope of such evidence. Relatedly, I have been informed that a nexus or connection between the merits of the claimed invention and the alleged evidence of secondary considerations is necessary. Specifically, I have been informed that the secondary considerations must be tied to purported novel or new elements of the claimed invention.

30. I also am informed that secondary considerations of nonobviousness include (1) whether the claimed subject matter achieved unexpected results or benefits, (2) whether the claimed subject matter satisfied a long-felt but unmet need, (3) whether the claimed subject matter was commercially successful as a result of the merits of a claimed subject matter (rather than the result of design needs, market pressure, advertising, or similar activities), (4) whether

other skilled artisans failed in their attempts to solve the same problems addressed by the invention, (5) whether others copied the claimed subject matter, and (6) whether others in the field praised claimed the subject matter.

31. Specifically, I am informed that evidence that other skilled artisans failed in their attempts to solve the same problems addressed by claimed invention is potential evidence of nonobviousness. To demonstrate failure of others, I am informed that plaintiff must establish that others skilled in the art tried and failed to find a solution for the problem allegedly solved by the invention claimed by the asserted patents. I further understand that for such evidence of failure to be relevant as an objective indicia of nonobviousness, these prior unsuccessful attempts must have failed because they lacked the claimed features of the asserted inventions. Purported failures unrelated to the patented invention are not relevant secondary considerations of nonobviousness.

32. I also am informed that evidence of a long-felt unmet need for the claimed invention is one factor courts may consider when assessing the obviousness of that invention. The underlying rationale for accepting evidence of a long-felt unmet need as evidence of nonobviousness, as I understand it, is based on the assumption that if an unmet need persists for a long time despite commercial incentives to offer a solution, the resolution of the problem may not be obvious. I also understand that the long-felt unmet need must be directly related to the subject matter of the claimed invention and must actually provide a result that meets the claimed need. I further am informed that the length of time that must pass to constitute a "long felt" need is to be determined in the light of the speed of innovation in the relevant industry. I also have been informed that long-felt, unmet need should be based upon alleged inadequacies in the technical knowledge of those skilled in the art, not due to business-driven market forces.

Lastly, I have been informed that any evidence of a need that post-dates the filing date of a challenged patent is irrelevant to the determination of nonobviousness.

33. I am further informed that "commercial success" is a legal construct that has been established through case law. I have been informed that analysis of commercial success is premised on the concept that if a product is economically successful, it may provide objective evidence of nonobviousness. I further understand that any purported commercial success of the product must be attributable to the alleged novel features of the claimed invention. I understand this to mean that, to support a finding of nonobviousness, any alleged commercial success must be driven by and attributable to the purported merits of the patented invention, and not by other factors unrelated to the allegedly novel features of the claimed invention. In other words, there must be a causal correlation, or "nexus," between the unique merit of the claimed invention and the success of the product. I also understand that if purported commercial success is due to an element in the prior art, no nexus exists.

34. I additionally understand that an alleged infringer's copying of a claimed invention rather than one that is in the public domain can support a finding of nonobviousness. Likewise, I am informed that to support a finding of nonobviousness, alleged industry praise must be linked to the patented invention. In other words, a patentee must show that any industry praise is attributable to material differences between the prior art and the patented invention. I have been informed that a patentee's statements that are intended to generate interest in a product are not evidence of industry praise. Similarly, publications authored or sponsored by or on behalf of a patentee fail to demonstrate true industry praise.

35. I further understand that the near simultaneous invention by two or more equally talented inventors working independently may or may not be an indication of obviousness. In

other words, the fact that another person simultaneously and independently created the same invention claimed in the patent-in-suit can serve as an indication that the invention was obvious.

C. Indefiniteness Under 35 U.S.C. § 112, ¶ 2

36. I have been informed that that 35 U.S.C. § 112, second paragraph, requires that a patent specification include claims particularly pointing out and distinctly claiming the subject matter which the inventor regards as his invention. I further understand that in order to comply with this requirement, a patent's claims, viewed in light of the specification and prosecution history, must inform those skilled in the art about the scope of the invention with reasonable certainty. Otherwise, the patent claims are invalid as indefinite.

37. I further have been informed that under this "reasonable certainty" standard, an undefined claim term renders a claim indefinite when it results in the existence of multiple methods leading to different results without guidance in the patent or the prosecution history. I also understand that this indefiniteness problem will persist even if someone skilled in the art could determine which method was the most appropriate.

38. I also understand that a claim may be indefinite where it employs a narrow numerical range that falls within a broader range, at least when the boundaries of the claim are not discernible. Likewise, I understand that claim language employing terms of degree may be indefinite where the language does not provide enough certainty to one of skill in the art when read in the context of the specification – for instance, where the term of degree is highly subjective and, on its face, provides little guidance to one of skill in the art such that, when combined with intrinsic evidence, the subjectivity does not provide a definition or boundaries for the term and/or does not provide any reference point for comparison.

D. Written Description Under 35 U.S.C. § 112, ¶ 1

39. I have been informed that the standard for satisfying written description with respect to a patent is that the patent specification reasonably conveys to a person having ordinary skill in the art that the inventor had possession of the subject matter of the claims as of the effective filing date.

E. Enablement Under 35 U.S.C. § 112, ¶ 1

40. I have been informed that to satisfy the enablement requirement with respect to a patent, the specification must describe the manner and process of making and using the claimed invention so as to enable the full scope of the claims, such that the public is enriched by the patent specification at least commensurate with the scope of those claims.

41. Furthermore, I understand that a patent specification that does not allow a person having ordinary skill in the art to practice the invention without undue experimentation is not enabled. I have been informed that certain factors are typically considered when evaluating the level of experimentation, such as the quantity of experimentation necessary to make or use the invention based on the content of the disclosure, the amount of direction or guidance presented by the inventor, the presence or absence of working examples, the breadth of the claims, the nature of the invention, the level of one of ordinary skill and the predictability or unpredictability of the art.

42. Therefore, I will analyze the prior art and other issues using this framework.

VI. LEVEL OF SKILL IN THE ART

43. I am informed and understand that the claims of a patent are judged from the perspective of a hypothetical construct involving a "person of ordinary skill in the art." The "art" is the field of technology to which the patent is related. I understand that the purpose of using the viewpoint of a person of ordinary skill in the art is for objectivity. I understand that a

person of ordinary skill in the art is presumed to know and be familiar with all of the relevant art in the field at the time of invention.

44. I was also asked to provide an opinion regarding the skill level of a person of ordinary skill in the art of the Family 3 patents. I considered several factors, including the types of problems encountered in the art, the solutions to those problems, the pace of innovation in the field, the sophistication of the technology, my experience as a person who worked in the art on the Family 3 patents' priority date, and the education level of active workers in the field.

45. In my opinion, at the time of the alleged invention, a person having ordinary skill in the art would have had a bachelor's degree in electrical engineering or computer engineering and 5 years of experience in digital communications, a Master's degree in electrical engineering and 2-3 years of experience in digital communications, or a Ph.D. in electrical engineering with 1-2 years of experience in digital communications.

46. I am qualified as a person of at least ordinary skill in the art, and my qualifications enable me to provide opinions regarding the Family 3 patents from the perspective of one of ordinary skill in the art.

VII. BACKGROUND OF THE TECHNOLOGY

47. The Family 3 patents share a common specification.[1] The Family 3 patents are generally directed to methods, systems, and apparatuses for allocating shared memory between interleavers and deinterleavers.

A. Forward Error Correction and Reed Solomon Coding

48. In a digital communication system, a transmitter transmits data to a receiver over a channel. The channel attenuates and adds noise to the transmitted signal. As a result,

[1] Accordingly, citations are to U.S. Patent No. 7,844,882 ("the '882 patent") unless otherwise noted.

sometimes the bits detected by the receiver do not match the bits represented by the transmitted signal sent by the transmitter. Consequently, digital communication systems often employ certain well-known techniques to detect, and sometimes correct, errors in the received bit stream.

49. Error correction techniques enable a receiver to detect the presence of errors and also correct at least some of those errors. To apply an error correction technique, the transmitter adds redundant information to a message to be transmitted. The receiver then uses the redundant information to detect a limited number of errors that may occur anywhere in the message, and often to correct those errors. When the communication system uses an error correction technique, the receiver can correct at least some errors in the received data, which reduces and could eliminate entirely any need for the receiver to request retransmission of corrupted messages.

50. Practical error correction techniques are often called forward error correction (FEC). One type of FEC is block codes. To apply a block code, the transmitter partitions the data to be transmitted into blocks and adds redundancy to each block to form a *codeword*. The transmitter appends r redundancy symbols to each block of k symbols, without altering the original k symbols, to form codewords having $k + r$ symbols. The receiver then uses the information in the r redundancy symbols to automatically detect and correct errors in the data portion of the codeword. A well-known example of a block code is the Reed-Solomon coding used in ADSL and VDSL.

51. Many communication systems, including ADSL and VDSL, are byte-oriented systems, and each Reed-Solomon-encoded data block contains an integer number of bytes. The bytes in each Reed-Solomon codeword include K data bytes (i.e., the data to be transmitted in

the block) and R redundancy bytes that result from the Reed-Solomon code calculation. Thus, the size of each Reed-Solomon codeword is N = K + R bytes long.

52. The mathematics of Reed-Solomon codes are complicated, but the essential property is that the maximum number of data elements with any number of errors that can be corrected is equal to half of the number of redundancy elements. In other words, a byte-oriented Reed-Solomon code can correct as many as R/2 errored data bytes, regardless of how many individual errors are within those data bytes.

53. As a simple example, if R = 16, up to 8 erroneous bytes can be corrected, regardless of how many bits of each errored byte are in error. Reed-Solomon codes are particularly helpful for use in environments that suffer from noise bursts because any erroneous element counts as a single error regardless of how many bits of that element are in error.

B. Interleaving and Deinterleaving

54. Interleaving is a technique used in ADSL and VDSL to improve the performance of Reed-Solomon coding in the presence of *impulse noise*, by which I mean intermittent and unpredictable bursts of noise that can temporarily overwhelm the data-carrying signal over several consecutive symbol periods. Deinterleaving is the complementary process that "undoes" interleaving. Interleaving—and, therefore, deinterleaving—have been specified in ADSL since the first T1.413 Issue 1 standard was published in 1995.

55. To apply interleaving, the transmitter shuffles consecutive bytes of the data stream in a known and systematic way before transmitting them to the receiver. As a result of the interleaving process, bytes that are adjacent in the data sequence are transmitted non-consecutively, spread out over a time interval. The receiver knows how the transmitter interleaved the bytes and reorders them before performing Reed-Solomon decoding to detect, and ideally correct, errors within the codewords.

56. Figure 1 below illustrates how the interleaving process works using a simple interleaving procedure. The transmitter separates the data elements into a number of blocks of five elements each (i.e., A1, A2, A3, A4, A5; B1, B2, B3, B4, B5; etc.). Elements from four blocks are then interleaved and transmitted in turn to create a sequence AxBxCxDx.

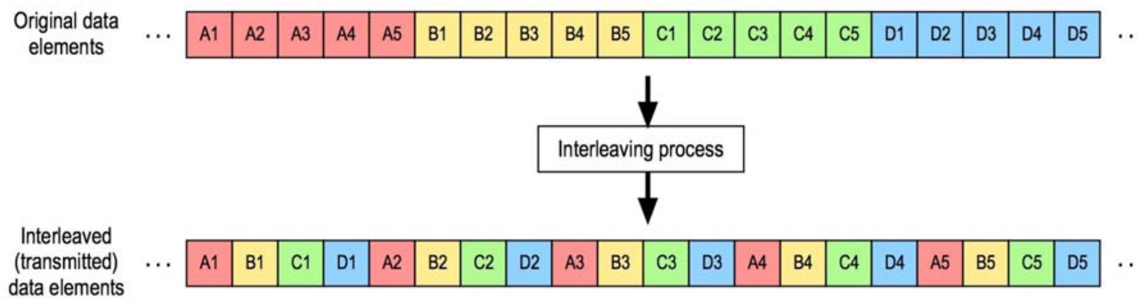

Figure 1: Interleaving example

57. Note that the interleaving process significantly increases the time interval over which the data elements from each of the individual data blocks are transmitted. Following the interleaving process in this simple example, the first and last data elements of each block are separated by 15 other data elements, and consecutive data elements of each block are separated by three other data elements. In real systems, the separation after interleaving will normally be hundreds or even thousands of bytes.

58. The receiver knows how the transmitter interleaved the data elements and can reverse the interleaving process by collecting all of the interleaved data elements and using a complementary deinterleaving process. The deinterleaving process results in the data elements being reordered into their original sequence, as shown in Figure 2 below.

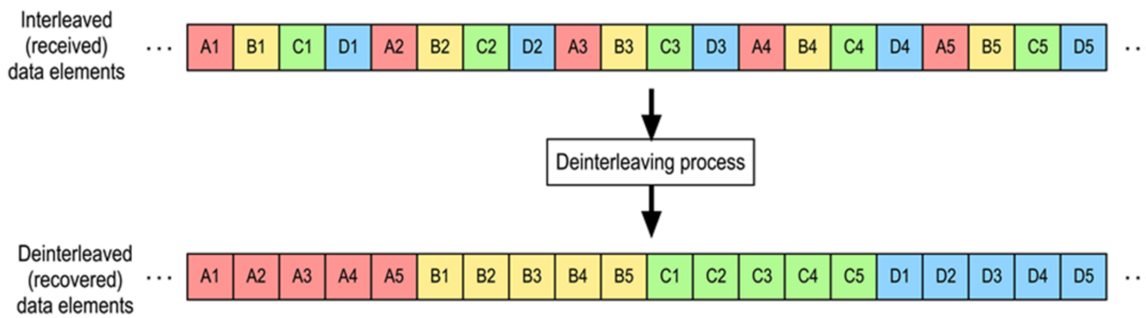

Figure 2: Deinterleaving example

59. DSL systems often use interleaving to improve the performance of the Reed-Solomon code. Errors in the received data caused by impulse noise tend to occur in bursts. Without interleaving, impulse noise causes errors that are concentrated within one or more consecutive Reed-Solomon codewords. As I explained above, a Reed-Solomon code can correct up to R/2 errored data elements in a codeword, where R is the number of redundancy bytes. If a single codeword has more than R/2 data bytes with errors, the Reed-Solomon code cannot correct all of the errors. Without interleaving, impulse noise can readily cause errors in more than R/2 of the bytes within a single Reed-Solomon codeword, which means the Reed-Solomon code (probably) cannot correct all of those errors.

60. If the transmitter interleaves the bytes prior to transmission, however, the effects of bursts of errors are spread out over multiple Reed-Solomon codewords when the bytes are reordered by the receiver, instead of being concentrated in a fewer number of Reed-Solomon codewords. After deinterleaving, the code can correct all of the errors as long as none of the reordered blocks of data bytes has more than R/2 bytes with errors.

61. As an example of the effects of impulse noise on Reed-Solomon coding effectiveness without interleaving, assume a transmitter sends a sequence of bytes as follows:

$$\left| B_0^1 \; B_1^1 \; B_2^1 \; B_3^1 \; B_4^1 \; B_5^1 \; B_6^1 \right| B_0^2 \; B_1^2 \; B_2^2 \; B_3^2 \; B_4^2 \; B_5^2 \; B_6^2 \left| B_0^3 \; B_1^3 \; B_2^3 \; B_3^3 \; B_4^3 \; B_5^3 \; B_6^3 \right| \cdots$$

where the subscripts are the byte indices within a codeword, and the superscripts are the codeword indices. The vertical lines show the codeword boundaries. Assume impulse noise corrupts five consecutive bytes as shown below by Xs:

$$\Big|\ B_0^1\ \ B_1^1\ \ B_2^1\ \ B_3^1\ \ B_4^1\ \ B_5^1\ \ B_6^1\ \Big|\ B_0^2\ \ B_1^2\ \ B_2^2\ \ B_3^2\ \ X\ \ X\ \ X\ \Big|\ X\ \ X\ \ B_2^3\ \ B_3^3\ \ B_4^3\ \ B_5^3\ \ B_6^3\ \Big|\cdots$$

Assuming R/2 is 2, the Reed-Solomon code can correct the two errored bytes in the third codeword, but it cannot correct each of the three errored bytes in the second codeword.

62. ADSL and VDSL use a particular kind of interleaving called *convolutional interleaving*. Figure 3 below is an example illustrating how a transmitter performs convolutional interleaving. Visualizing the interleaver memory as a matrix, codewords are written into the rows and read out of the columns of the matrix to create the interleaved stream of bytes. In convolutional interleaving, the first bytes of the D codewords in different rows are in different columns (i.e., subsequent codewords are shifted to the right by one column when written into the rows). The deinterleaver operates similarly to the interleaver, except that the received bytes are written into the columns of the matrix and read out row by row.

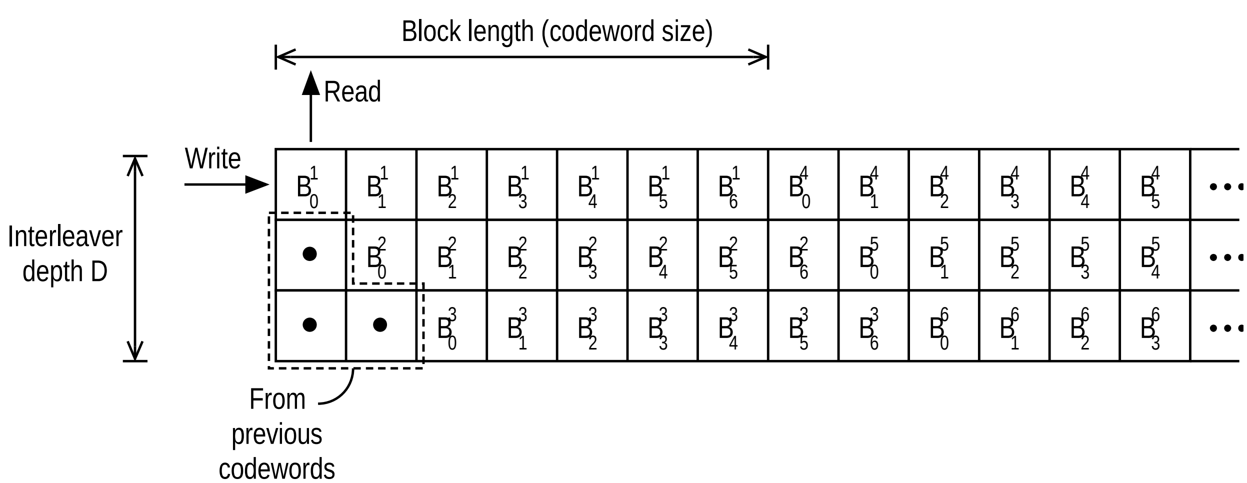

Figure 3: Convolutional interleaver with 7-byte codeword length and depth D = 3

63. In the example of Figure 3, the interleaver depth D is 3 bytes, and the codeword size I is 7 bytes. The large dots within the squares at the left-hand side of the figure represent bytes from previous codewords. To help with visualization of how convolutional interleaving works, the rows are depicted as never ending so that additional codewords can be added to each of the rows in sequence.

64. In order of left to right, the interleaved stream for the example convolutional interleaver shown in Figure 3 is

$$B_0^1 \quad \bullet \quad \bullet \quad B_1^1 \quad B_0^2 \quad \bullet \quad B_2^1 \quad B_1^2 \quad B_0^3 \quad B_3^1 \quad B_2^2 \quad B_1^3 \quad B_4^1 \quad B_3^2 \quad B_2^3 \quad B_5^1 \quad B_4^2 \quad B_3^3 \quad B_6^1 \quad B_5^2 \quad B_4^3 \cdots$$

The bytes that were adjacent in the original data stream are separated by 3 bytes (the interleaver depth D) after interleaving.

65. Now if impulse noise corrupts the five consecutive bytes in the same location as shown above, the resulting interleaved stream of bytes is:

$$B_0^1 \quad \bullet \quad \bullet \quad B_1^1 \quad B_0^2 \quad \bullet \quad B_2^1 \quad B_1^2 \quad B_0^3 \quad B_3^1 \quad B_2^2 \quad X \quad X \quad X \quad X \quad X \quad B_4^2 \quad B_3^3 \quad B_6^1 \quad B_5^2 \quad B_4^3 \cdots$$

When the bytes are deinterleaved, the resulting stream of codewords is:

$$\left| B_0^1 \quad B_1^1 \quad B_2^1 \quad B_3^1 \quad X \quad X \quad B_6^1 \right| B_0^2 \quad B_1^2 \quad B_2^2 \quad X \quad B_4^2 \quad B_5^2 \quad B_6^2 \left| B_0^3 \quad X \quad X \quad B_3^3 \quad B_4^3 \quad B_5^3 \quad B_6^3 \right| \cdots$$

After the bytes have been returned to their original order, no codeword includes more than two bytes in error, and the Reed-Solomon code can correct all of the errors.

66. The process of interleaving in the transmitter and deinterleaving in the receiver introduces delay (or latency) because bytes are stored for a period of time after they are written to the interleaver or deinterleaver memory but before they are read out. All bytes have the same total delay between the input to the interleaver and the output of the deinterleaver, which is typically referred to as the *end-to-end interleaver delay* (with the understanding that the delay contributed by the deinterleaving process is included, too). In units of time, the end-to-end

interleaver delay depends on the rate at which the transmitter transmits bytes, i.e., the bit rate over the communication channel in the downstream direction, because that rate determines how quickly the transmitter processes the bytes for transmission.

67. The amount of memory needed for convolutional interleaving depends on how the interleaver and deinterleaver are implemented. The minimum amount of memory required for a convolutional interleaver and deinterleaver pair is $(D-1) \times (I-1)$ bytes.

68. The primary penalties for including interleaving in a communication system are increased latency (due to the end-to-end interleaver delay) and a requirement for additional memory in both the transmitter and receiver. The end-to-end interleaver delay increases with the interleaver depth. Therefore, there is a fundamental trade-off between latency and improved Reed-Solomon performance. A larger interleaver depth offers better potential to improve the performance of the Reed-Solomon coding but also increases latency.

C. Shared Memory

69. As I explain further in the prior art discussion below, the idea of a transceiver sharing a common memory for interleaving and deinterleaving was well known as of the Family 3 patents' priority date.

70. For convenience, I will sometimes distinguish in this report between a "near-end" transceiver and the "far-end" transceiver that is on the other side of a communication channel from the near-end transceiver. When the transmitter of a near-end transceiver performs interleaving, the transmitter needs to have access to an amount of memory sufficient for the transmitter to perform the interleaving procedure. Likewise, when the transmitter in the far-end transceiver performs interleaving, the near-end transceiver's receiver must have access to an amount of memory sufficient to enable it to deinterleave the data interleaved by the far-end transceiver's transmitter. And, of course, the far-end transceiver needs sufficient memory to

deinterleave the data transmitted by the near-end transmitter and to interleave the data it is transmitting to the near-end receiver.

71. There are two ways to provide the memory needed for a transceiver's interleaving and deinterleaving procedures. The first way is to provide a specified amount of dedicated interleaver memory and a specified amount of dedicated deinterleaver memory. The transmitter has exclusive access to the interleaver memory and can, at least in theory, use as much as all of the interleaver memory for interleaving. Similarly, the receiver has exclusive access to the deinterleaver memory and can, at least in theory, use as much as all of the deinterleaver memory for deinterleaving.

72. The second way to meet the transceiver's memory requirements for interleaving and deinterleaving is to provide shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis. Use of a shared memory for interleaving and deinterleaving, including in DSL, was well known before the priority date of the Family 3 patents. *See, e.g.*, U.S. Patent Pub. No. 2005/0034046 by Berkmann *et al.* at Abstract (disclosing a "combined interleaving and deinterleaving circuit" with "data memory (RAM) for temporary storage of the data to be interleaved and deinterleaved"); U.S. Patent No. 6,707,822 to Fadavi-Ardekani *et al.* at Abstract (disclosing an "Interleave/De-Interleave Memory" that "is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session"); U.S. Patent No. 6,381,728 to Kang at col. 5:35-38 (disclosing "double buffering [that] allows the channel interleaver memory to be used, along with the app memory, as the turbo deinterleaver memory"); U.S. Patent No. 7,269,208 to Mazzoni *et al.* at Abstract (disclosing memory having "a first memory space assigned to the interleaver and a second memory space assigned to the deinterleaver"); *id.* at col. 1:19-22 ("The present

invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system. . . ."); U.S. Patent No. 5,751,741 to Voith *et al.* at col. 4:47-50 (disclosing external interleave/deinterleave memory used by both transmitter for interleaving and receiver for deinterleaving); *id.* at col. 2:61-64 ("Generally, the present invention provides an ADSL transceiver. . . .").

73. Once the shared memory has been partitioned between the transmitter's interleaver and the receiver's deinterleaver for a connection, the transmitter has exclusive access to the portion of the shared memory allocated for interleaving and can, at least in theory, use as much as all of that portion of the shared memory for interleaving. Similarly, the receiver has exclusive access to the portion of the shared memory allocated for deinterleaving and can, at least in theory, use as much as all of that portion of the shared memory for deinterleaving. When the connection terminates, the shared memory can thereafter be repartitioned, possibly differently, when new connections are established.

74. Because the interleaving procedure is performed by one transceiver, and the corresponding deinterleaving procedure is performed by a different transceiver, it is necessary for at least one of the transceivers to know the capabilities or requirements of the other transceiver in order to configure the interleaver (or deinterleaver). Otherwise, for example, the transceiver performing the interleaving procedure could use an interleave depth that requires more memory than is available to the transceiver performing the deinterleaving procedure.

75. For example, before the near-end transceiver can configure its interleaver, which establishes how much of the memory available for interleaving (in either a dedicated memory or shared memory) the transmitter will use, it needs to know something about the far-end transceiver's deinterleaving capabilities; otherwise, the near-end transmitter could perform an

interleaving procedure that the far-end receiver is incapable of reversing (e.g., because it does not have sufficient memory). In addition, before the near-end transceiver can configure its deinterleaver, which establishes how much of the memory available for deinterleaving (in either a dedicated memory or shared memory) the receiver will use, it needs to know how the far-end transceiver will be interleaving the data; otherwise, the near-end receiver will be unable to perform the corresponding deinterleaving procedure.

76. As discussed below, since 1995, the ADSL and VDSL standards have provided for the near-end and far-end transceivers to communicate their interleaving requirements and/or capabilities to each other during an initialization procedure.

D. Latency Paths

77. Different types of data have different levels of sensitivity to delays that occur during transmission. For example, real-time voice data, such as from a telephone call, cannot tolerate large delays because delays in conversations are very annoying for the participants. In contrast, a pre-stored (i.e., non-real-time) video transmitted to a receiver (e.g., via YouTube, Netflix, HBO Go, etc.) can tolerate a substantial amount of delay because the local video playback device typically buffers at least some of the video before playing it.

78. To enable the transmission of both delay-sensitive and delay-tolerant data over the same subscriber line, the ADSL and VDSL standards, discussed below, define multiple *latency paths* that allow a single DSL connection to transfer multiple types of data having different latency requirements (or delay tolerances) at the same time. Each latency path is characterized by a distinct delay (or latency), which may be the same as or different from the delay(s) of other latency paths. For example, one latency path may be characterized by a relatively large delay because of interleaving in the transmitter and deinterleaving in the

receiver, whereas another latency path may be characterized by a relatively small delay because of little or no interleaving.

79. The delay of a particular latency path depends on the FEC and interleaving used in that path. For example, when a latency path includes both FEC and interleaving, the delay depends on the codeword size and the interleave depth.

E. Overview of DSL Standards Groups

80. Many of the aspects of ADSL and VDSL have been standardized by standard-setting organizations (SSOs), such as the Alliance for Telecommunications Industry Solutions (ATIS) and the International Telecommunications Union (ITU). This section introduces two of the working groups and the standards they produced that are relevant to the subject matter of this case and pre-date the priority date of the Family 3 patents. It also provides a brief overview of how the work in the responsible working groups is conducted.

1. T1E1.4

81. The earliest standardization work in ADSL was undertaken in the United States by the T1E1.4 technical subcommittee of Committee T1, a telecommunications standards body sponsored by ATIS and accredited by the American National Standards Institute (ANSI).

82. In 1995, ATIS published the world's first ADSL standard, T1.413. I will refer to the first version of the T1.413 standard herein as "T1.413 Issue 1." In 1998, ATIS published a revision of T1.413, which I will refer to as "T1.413 Issue 2." Both T1.413 Issue 1 and T1.413 Issue 2 specify the required operations of ADSL transceivers (referred to as the "ATU-C" and "ATU-R").

83. After releasing T1.413 Issue 2 ADSL, T1E1.4 focused less on developing stand-alone transceiver standards and more on providing inputs to the ITU-T, discussed below, regarding North American requirements and preferences for emerging DSL standards.

2. ITU-T Study Group 15, Question 4

84. In 1997, the Telecommunications Sector of the ITU, known as the ITU-T, also began working on ADSL standardization. The ITU-T generates standards called "Recommendations" for all fields of telecommunications. Recommendations are the result of work by members of the ITU-T, which include Member States (e.g., the United States and other members of the United Nations), Sector Members, and Associates. Sector Members and Associates are generally companies and other organizations.

85. DSL standardization is carried out by Study Group 15 of the ITU-T. The work of Study Group 15 is partitioned into work areas known as "Questions." DSL standardization work takes place within Study Group 15, Question 4 (abbreviated herein as "SG15/Q4"). SG15/Q4 became the primary group responsible for defining DSL transceiver standards after T1E1.4 completed T1.413 Issue 2.

86. The ITU-T's DSL Recommendations are primarily aimed at defining mandatory and optional functions of DSL transceivers. In 1997, among other projects, SG15/Q4 established the projects known as "G.dmt" and "G.lite." At that time, T1.413 Issue 1 was in force, and T1E1.4 was developing what eventually became T1.413 Issue 2 ADSL. G.dmt was expected essentially to adopt T1.413 Issue 2 and add annexes addressing country-specific requirements. The work in G.dmt was eventually released in 1999 as ITU-T Recommendation G.992.1, entitled "Asymmetric digital subscriber line (ADSL) transceivers," much of which is identical to T1.413 Issue 2. G.992.1 specifies requirements for both the ATU-C and the ATU-R to enable connections that support at least 6.144 Mbit/s in the downstream direction (i.e., toward the subscriber, from the ATU-C to the ATU-R) and at least 640 kbit/s in the upstream direction (i.e., away from the subscriber, from the ATU-R to the ATU-C) without interfering with "plain old telephone signals" (POTS) on the same subscriber line.

87. G.lite was intended to be a lower-speed version of ADSL. The work in G.lite was eventually released, also in 1999, as ITU-T Recommendation G.992.2, entitled "Splitterless asymmetric digital subscriber line (ADSL) transceivers." Unlike G.992.1, which was designed to maximize performance, G.992.2 was designed to provide lower bit rates (i.e., a maximum of 1.536 Mbit/s downstream and 512 kbit/s upstream) by simplifying various aspects of the ATU-C and ATU-R.

88. After completing G.992.1, SG15/Q4 almost immediately began work on a revision, standardized in Recommendation G.992.3, entitled "Asymmetric digital subscriber line transceivers 2 (ADSL2)," the first version of which was approved in 2002. G.992.3 builds on many of the aspects of G.992.1 to enable connections that support at least 8 Mbit/s downstream and at least 800 kbit/s upstream.

89. In parallel with the work on ADSL2, SG15/Q4 also worked on a higher speed version of ADSL, known as ADSL2+. Recommendation G.992.5, entitled "Asymmetric Digital Subscriber Line (ADSL) transceivers – Extended bandwidth ADSL2 (ADSL2+)," was first approved in 2003. It specifies the physical layer characteristics of an ADSL transceiver that transmits over a wider bandwidth than an ADSL2 transceiver. G.992.5 is defined in a "delta document" to G.992.3, meaning that it incorporates the content of G.992.3 and specifies only changes and additions to that document. As compared to G.992.3, G.992.5 enables transceivers to transmit using twice as much bandwidth in the downstream direction to provide at least 16 Mbit/s in the downstream direction and at least 800 kbit/s in the upstream direction.

90. In June of 2004, the ITU-T's first VDSL Recommendation, G.993.1, entitled "Very high speed digital subscriber line transceivers," was approved. It specifies transceiver

requirements to support the transmission of asymmetric and symmetric aggregate data rates up to tens of Mbit/s on twisted pairs.

3. Operation of DSL Standards Meetings

91. Both T1E1.4 and SG15/Q4 met regularly, typically 4 to 6 times per year, to begin work on new DSL standards, to discuss and improve the draft standards being developed at the time, and eventually to submit the standards for formal approval. In order to develop and improve the standards, T1E1.4 and SG15/Q4 participants submitted documents, referred to as "contributions." A contribution might identify a problem with an in-force standard and propose a solution for incorporation in a revision of that standard, or it might propose a new feature for a standard being developed, or it might propose to begin work on a new standard.

92. Each T1E1.4 contribution was assigned a unique identifier of the form "T1E1.4/YY-NNN" or "T1E1.4/YYYY-NNN," where "YY" or "YYYY" indicates the year, and "NNN" is a unique 3-digit number. The unique 3-digit number would reset to 001 at the beginning of each year. Each SG15/Q4 contribution is assigned a unique identifier of the form "MM-NNN," where "MM" is a 2-letter designator reflecting the location of the meeting (e.g., "DC" stands for "Durango, Colorado," "LB" stands for "Leuven, Belgium," etc.), and "NNN" is a unique 3-digit number. The unique 3-digit number resets to 001 for each SG15/Q4 meeting.

93. One unique aspect of T1E1.4, relative to many other SSO working groups, was that prior to 2004, its meetings were open to members of the public, and the contributions distributed to meeting participants and/or posted on Committee T1's website were freely available to the public without any distribution restrictions. Thus, any member of the public could attend T1E1.4 meetings free of charge and obtain copies of the contributions submitted to that meeting. Members of the public could also download contributions from Committee T1's website. Meetings of T1E1.4 were typically held in the United States.

94. SG15/Q4 meetings were (and are) open to and attended by members of the ITU-T. ITU-T membership was (and is) available to interested companies and organizations for an annual fee that, as of June of 2004, was 10,500 Swiss francs.[2] I personally attended SG15/Q4 meetings starting in 2000,[3] and I recall the meetings being attended by most of the companies developing DSL chips and transceivers, as well as the service providers deploying DSL.[4]

F. Interleaving and FEC in DSL Standards

95. As explained above, interleaving and FEC, and specifically the use of Reed-Solomon coding, have been specified for ADSL since the first ADSL standard, T1.413 Issue 1, was completed in 1995. Each of the subsequent ADSL and VDSL standards released before the Family 3 patents' priority date also specifies interleaving, FEC, and protocols to enable the near-end and far-end transceivers to inform each other of their capabilities and/or requirements during the initialization procedure.

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[2] *See* https://web.archive.org/web/20040603123217/http://www.itu.int:80/ITU-T/membership/associates.html (last visited November 16, 2018).

[3] I attended SG15/Q4 on behalf of Texas Instruments until May of 2004 and on behalf of 2Wire from August of 2004 through June of 2006.

[4] According to the Internet Archive, as of December 6, 2000 the ITU-T members included, among others: 3Com, ADTRAN, Alcatel, Analog Devices, AT&T, Aware, Bell Atlantic, Bell Canada, Bell South, Broadcom, British Telecom, Burr-Brown Corporation, Catena Networks, Centillium Communications, Cisco Systems, Conexant Systems, Copper Mountain Networks, Covad Communications, Element 14, Ericsson, Excess Bandwidth Corporation, France Telecom, Fujitsu, Globespan, Infineon, Italtel, Legerity, Level One, LG Electronics, Lucent, Marconi Communications, Matsushita, Metalink, Mitel Corporation, Mitsubishi, Motorola, NEC, Next Level Communications, Nokia, Nortel Networks, NTT, PairGain, Paradyne Corporation, Philips, PMC-Sierra, Qwest, Sagem, Sasken, SBC Communications, Siemens, Sprint, STMicroelectronics, Sumitomo, Swisscom, Telcordia, Telecom Italia, Telenor, Telesis Technologies Laboratory, Telia, Tellabs, Texas Instruments, VDSL Systems, Verizon, Velocity Communication (later renamed Ikanos), and Virata. *See* https://web.archive.org/web/20001206175700/http://www.itu.int:80/cgi-bin/htsh/mm/scripts/mm.list?_search=SEC%26_languageid=1 (last visited November 16, 2018).

1. Nomenclature

96. In ADSL, one transceiver is located on the service provider's side of the subscriber line, often in the service provider's central office (CO), and the other transceiver is located on the customer's side of the subscriber line. The ADSL transceiver located on the service provider's side of the subscriber line is referred to as the "ATU-C," and the ADSL transceiver located on the customer's side of the subscriber line is referred to as the "ATU-R."

97. In VDSL, one transceiver is located on the service provider's side of the subscriber line, potentially in an optical network unit (ONU), and the other transceiver is located on the customer's side of the subscriber line. The VDSL transceiver located on the service provider's side of the subscriber line is referred to as the "VTU-O," and the VDSL transceiver located on the customer's side of the subscriber line is referred to as the "VTU-R."

98. The direction of transmission from the ATU-C (or VTU-O) to the ATU-R (or VTU-R) is the *downstream* direction, and the direction of transmission from the ATU-R (or VTU-R) to the ATU-C (or VTU-O) is the *upstream* direction.

99. If interleaving is used in both the upstream and downstream directions in ADSL, both the ATU-C and ATU-R use both an interleaver and a deinterleaver. The ATU-R interleaves upstream data (for transmission to the ATU-C) and deinterleaves downstream data (interleaved by and received from the ATU-C). Conversely, the ATU-C interleaves downstream data (for transmission to the ATU-R) and deinterleaves upstream data (interleaved by and received from the ATU-R).

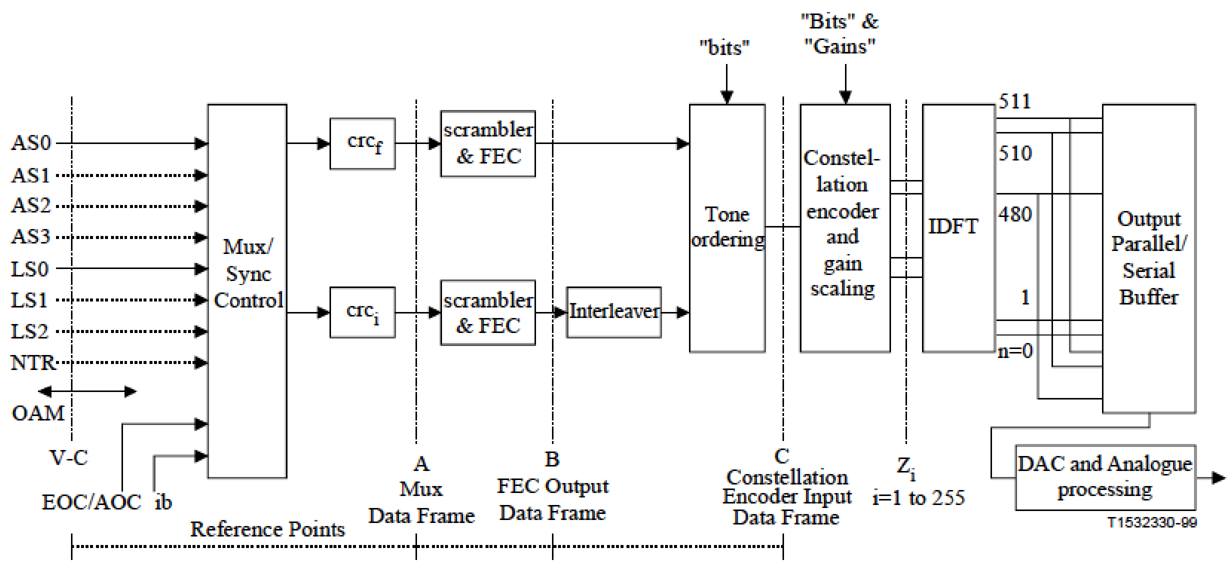
100. Similarly, in VDSL, if interleaving is used in both the upstream and downstream directions, both the VTU-O and VTU-R use both an interleaver and a deinterleaver. The VTU-R interleaves upstream data (for transmission to the VTU-O) and deinterleaves downstream data (interleaved by and received from the VTU-O). Conversely, the VTU-O interleaves

downstream data (for transmission to the VTU-R) and deinterleaves upstream data (interleaved by and received from the VTU-R).

2. G.992.1 (1999)

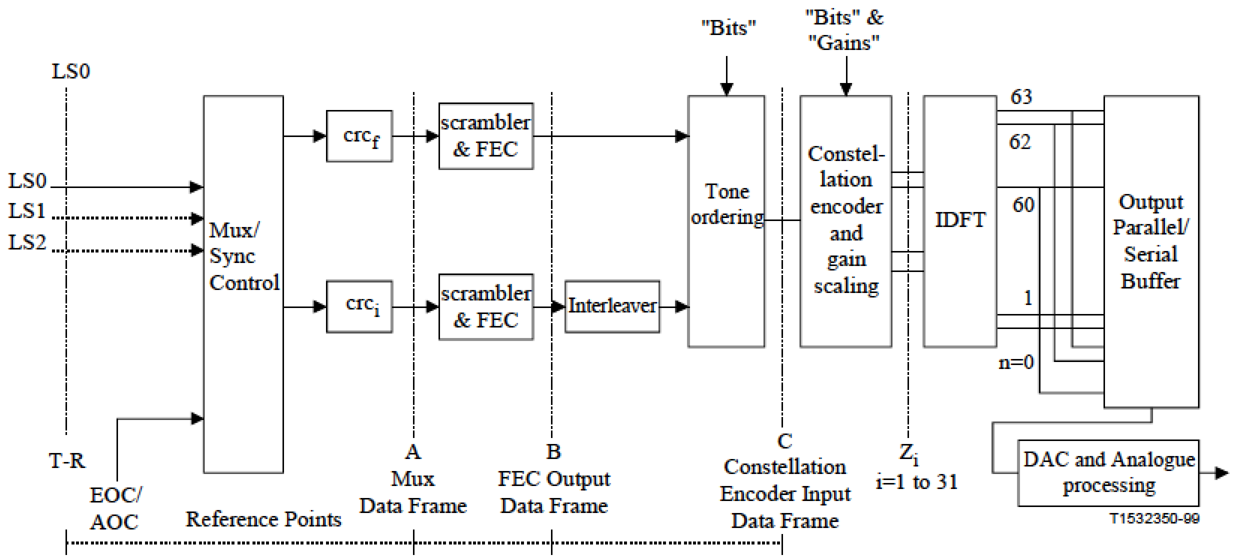
101. G.992.1 specifies dual-latency configurations using two independent data paths in both the downstream and upstream directions. G.992.1 also supports a single-latency configuration, which may include interleaving.

102. Figure 5-1 of G.992.1, copied below, is a reference diagram for the ATU-C, and Figure 5-3 of G.992.1, also copied below, is a reference diagram for the ATU-R.



NOTE – Solid versus dashed lines are used to indicate required versus optional capabilities respectively. This figure is not intended to be complete in this respect, see clauses 6 and 7 for specific details.

Figure 5-1/G.992.1 – ATU-C transmitter reference model for STM transport



NOTE – Solid versus dashed lines are used to indicate required versus optional capabilities respectively. This figure is not intended to be complete in this respect, see clauses 6 and 8 for specific details.

Figure 5-3/G.992.1 – ATU-R transmitter reference model for STM transport

In the downstream direction, there are up to two latency paths (fast and interleaved), and in the upstream direction there are also up to two latency paths (fast and interleaved), resulting in a total of four possible latency paths overall. When a single latency path is supported in one of the directions of transmission, it may use either the fast or interleaved path.

103. The key difference between the fast and interleaved paths in G.992.1 is that data in the interleaved path is both FEC encoded (using Reed-Solomon coding) and interleaved, as described previously, to improve the effectiveness of the FEC code in the presence of impulse noise. In contrast, the fast path includes FEC coding, but does not include interleaving. Therefore, the fast path has lower latency than the interleaved path, but it is also more likely to suffer from a higher error rate in the presence of impulse noise.

104. Each FEC codeword has a length of some number of bytes (i.e., N, K, and R all have units of bytes), which can be different for the fast and interleaved paths and in the downstream and upstream directions. The value of K depends on the transmitted bit rate (i.e.,

the rate at which the transmitter sends bits to the receiver on the other side of the subscriber line). The values of N, K, and R are set during the initialization procedure (with N = K + R).

105. G.992.1 specifies the interleave depth for the interleaved path as a number of FEC codewords.

106. During the initialization procedure, the ATU-C transmits four options for data rates and formats to the ATU-R using a signal known as "C-RATES1." Each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.1 at § 10.6.2. The ATU-R responds by transmitting a signal known as "R-RATES1," in which the ATU-R echoes the four options in the order in which the ATU-R prefers them. G.992.1 at § 10.7.4.

107. Figure 10-4 of G.992.1, copied below, shows the timing of the messages transmitted by the ATU-C and ATU-R during the "exchange" phase of initialization, which follows the transmission of the C-RATES1 and R-RATES1 messages.

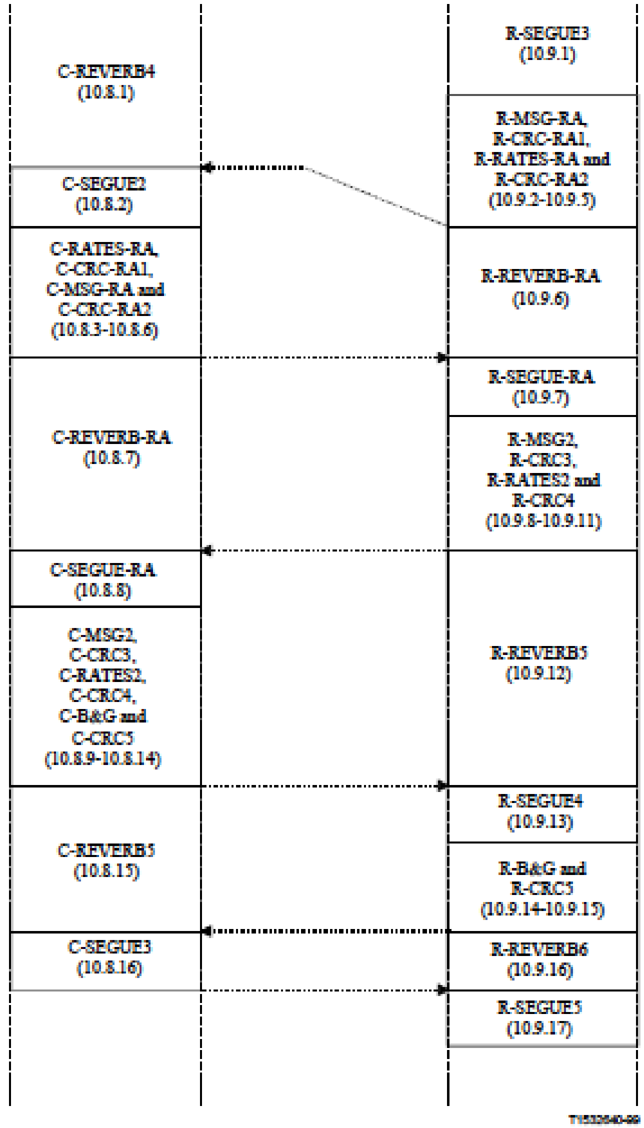


Figure 10-4/G.992.1 – Timing diagram of exchange

108. After transmitting R-RATES1 and measuring the signal-to-noise ratio (SNR) of the downstream channel, the ATU-R transmits a signal called "R-MSG-RA," which tells the ATU-C, among other things, the maximum interleave depth the ATU-R can support. G.992.1 at §§ 10.9.2, 10.9.2.7. The ATU-R also transmits a signal called "R-RATES-RA," which indicates either (a) the option number of the highest data rate from C-RATES1 that can be supported based on the measured SNR in the downstream direction, (b) no option selection was made but will be made later based on information in the C-RATES-RA signal the ATU-C will

transmit, or (c) the ATU-R cannot implement any of the options received in C-RATES1. G.992.1 at § 10.9.4.

109. After receiving R-MSG-RA and R-RATES-RA, the ATU-C transmits a signal called "C-RATES-RA," which sends four new options for data rates and formats for both upstream and downstream transmission. G.992.1 at § 10.8.3. As in C-RATES1, each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.1 at § 10.8.3.

110. After receiving C-RATES-RA, the ATU-R transmits R-RATES2, which selects only the number of the option with the highest data rate that can be supported in the downstream direction based on the ATU-R's measurements of the channel. G.992.1 at § 10.9.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.1 at § 10.8.11. The ATU-C's decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C's measurements of the channel. G.992.1 at § 10.8.11.

3. <u>G.992.2 (1999)</u>

111. G.992.2 specifies requirements and functions of ADSL transceivers intended to operate without the splitter filters required in G.992.1 to isolate ADSL signals from telephony signals on the same subscriber line. G.992.2 at Summary. Figure 2 of G.992.2, copied below, is the reference model for G.992.2 transmitters (both ATU-C and ATU-R).

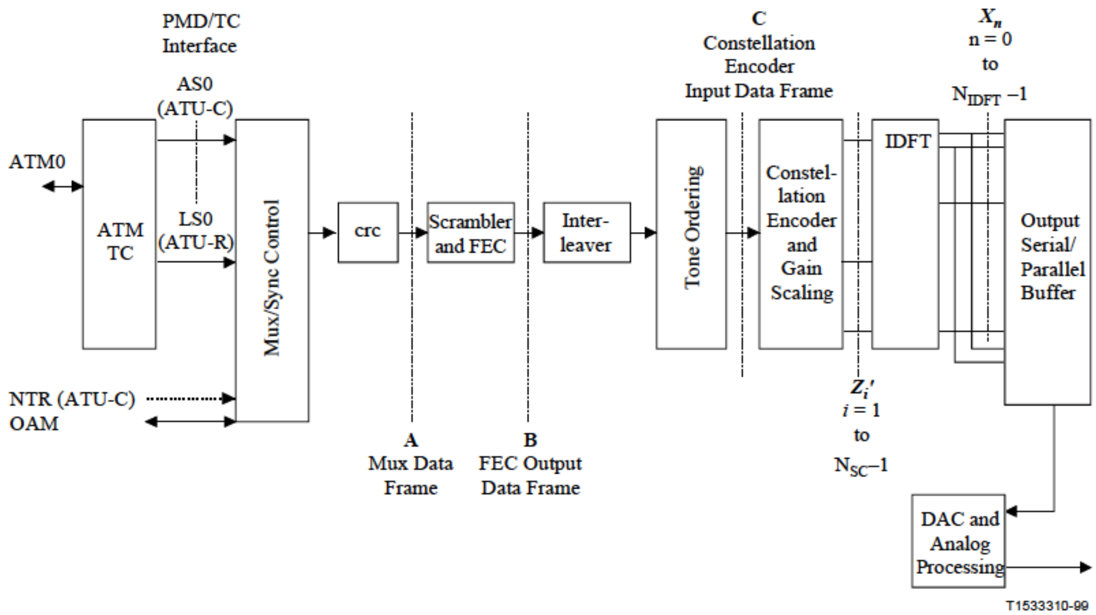


Figure 2/G.992.2 – ATU reference transmitter model

112. G.992.2 is similar to G.992.1 in how it handles the selection and communication of FEC and interleaver settings during the initialization procedure. The ATU-C transmits C-RATES1, which contains four options, in order of decreasing preference, for downstream and upstream data rates and formats. G.992.2 at § 11.9.2. Each option contains Reed-Solomon FEC and interleaver parameters, such as the downstream interleave depth in codewords. G.992.2 at § 11.9.2. The ATU-R responds by sending R-RATES1, in which the ATU-R echoes the four options received from the ATU-C in order of decreasing preference. G.992.2 at § 11.10.4.

113. Figure 26 of G.992.2, copied below, shows the "exchange" phase of initialization, which takes place after the ATU-C and ATU-R have transmitted, respectively, C-RATES1 and R-RATES1.

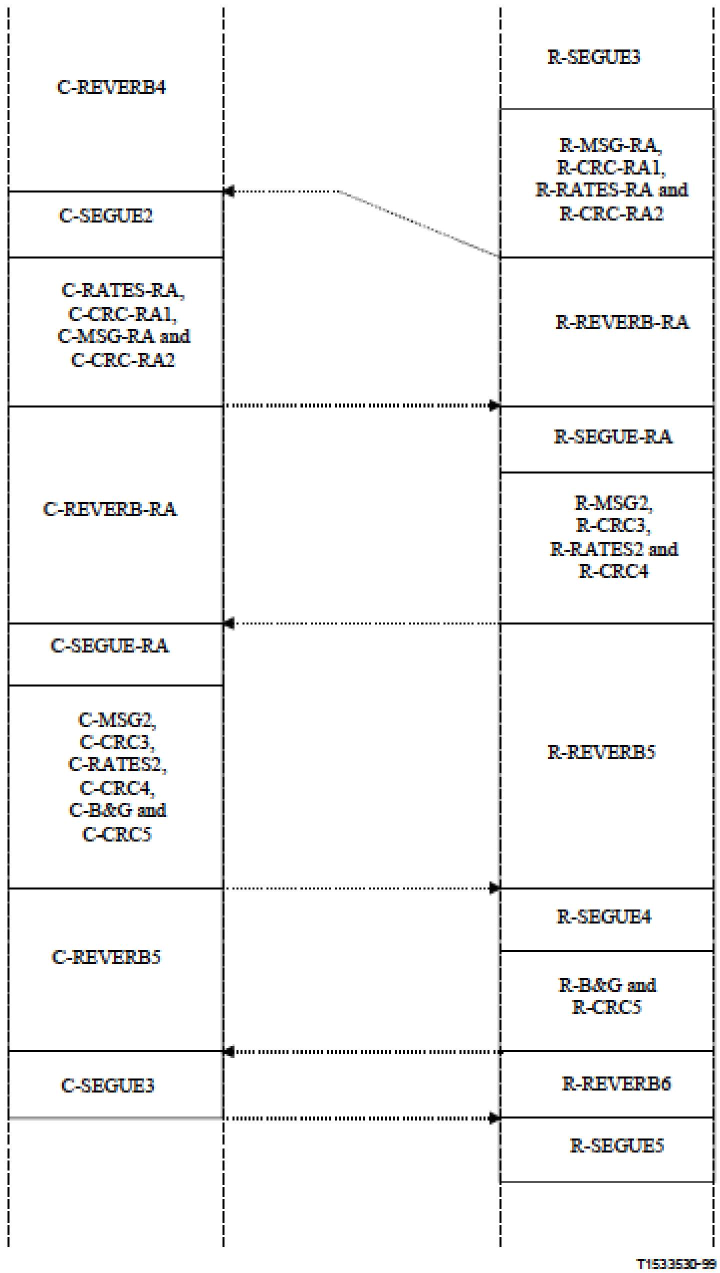


Figure 26/G.992.2 – Timing diagram of exchange

114. After assessing the channel, the ATU-R sends R-MSG-RA, which includes, among other things, a number of Reed-Solomon overhead bytes (R) and a number of Reed-Solomon payload bytes (K). G.992.2 at § 11.12.2. The ATU-R also sends R-RATES-RA, which indicates either (a) the option number of the highest data rate sent in C-RATES1 that can be supported based on the measured SNR in the downstream direction, (b) no option selection

was made but will be made later based on information in the C-RATES-RA signal the ATU-C will transmit, or (c) the ATU-R cannot implement any of the options received in C-RATES1. G.992.2 at § 11.12.4.

115. The ATU-C then transmits C-RATES-RA, which contains four new options for data rates and formats for both upstream and downstream transmission. G.992.2 at § 11.11.3. As in C-RATES1, each of the options includes downstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-C proposes to do for each option) and upstream FEC settings and an interleave depth in FEC codewords (i.e., to notify the ATU-R of the FEC coding and interleaving the ATU-R will need to do for each of the options). G.992.2 at § 11.11.3.

116. In response to C-RATES-RA, the ATU-R transmits R-RATES2, which selects only the number of the option with the highest data rate that can be supported in the downstream direction based on the ATU-R's measurements of the channel. G.992.2 at § 11.12.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.2 at § 11.11.11. The ATU-C's decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C's measurements of the channel. G.992.2 at § 11.11.11.

4. G.993.1 (2004)

117. ITU-T Recommendation G.993.1 specifies aspects of very high-speed digital subscriber lines (VDSL) to permit the transmission of asymmetric and symmetric aggregate data rates up to tens of Mbit/s on twisted pairs. G.993.1 provides for use of a wider bandwidth than is used in ADSL, namely, up to 12 MHz. G.993.1 at § 1.

118. Among other things, G.993.1 specifies the use of FEC and interleaving in the transmitter. Figure 8-1 of G.993.1, copied below, illustrates the defined "slow" and "fast" paths. As shown, the "slow" path includes both FEC and interleaving, whereas the "fast" path includes FEC but not interleaving.

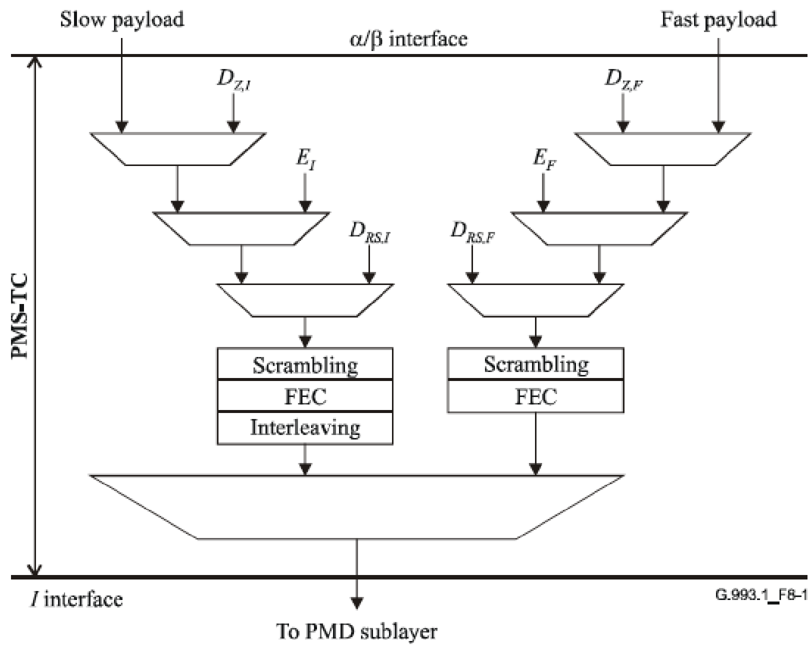


Figure 8-1/G.993.1 – Diagram of PMS-TC sublayer

119. G.993.1 specifies the use of "a standard byte-oriented Reed-Solomon code . . . to provide protection against random and burst errors" (G.993.1 at § 8.3) and interleaving "to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords." G.993.1 at § 8.4.1. Specifically, "the codewords shall be interleaved before transmission to increase the immunity of RS [Reed-Solomon] codewords to bursts of errors." G.993.1 at § 8.4.1. The interleave depth is programmable up to a maximum depth of 64 codewords when the codeword length is 255 bytes. *Id.* When the codeword is shorter than 255 bytes, the interleave depth can be larger than 64 codewords. *Id.*

120. G.993.1 specifies that "[i]t shall be possible to adjust the interleave depth via the management system to meet latency requirements." *Id.* The interleaver "uses a memory in which a block of I octets is written while an (interleaved) block of I octets is read." *Id.* G.993.1 teaches that the receiver requires the same size of memory for deinterleaving as the transmitter uses for interleaving. *Id.*

121. G.993.1 specifies an initialization procedure to allow the VTU-O and VTU-R to, among other things, exchange parameters such as Reed-Solomon settings and interleaver parameters. G.993.1 at § 12.4.1. Figure 12-7 of G.993.1, copied below, illustrates the timing of messages transmitted by the VTU-O and VTU-R during the channel analysis and exchange phase of VDSL initialization.

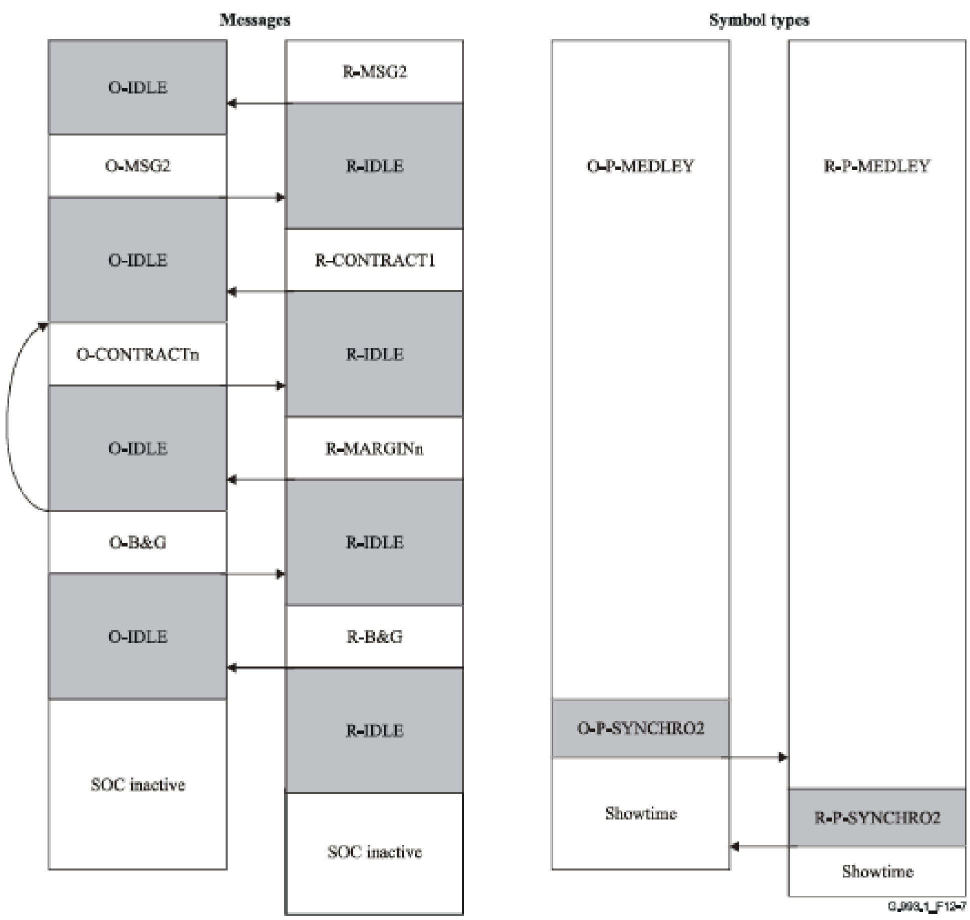


Figure 12-7/G.993.1 – Timeline of the channel analysis and exchange phase

122. During the channel analysis and exchange phase, the VTU-R sends a message called R-MSG2, which transfers, among other things, the Reed-Solomon capabilities of the VTU-R (e.g., whether it can support only mandatory settings or all settings), the interleaver settings supported by the VTU-R (e.g., whether it can support only mandatory settings, all settings, or a number of additional settings), and the "maximal interleaver memory" in bytes. *Id.*at § 12.4.6.1; § 12.4.6.3.1.1.

123. After receiving R-MSG2, the VTU-O sends a message called O-MSG2, which transfers, among other things, the Reed-Solomon capabilities of the VTU-O (e.g., whether it can support only mandatory settings or all settings), the interleaver settings supported by the VTU-O (e.g., whether it can support only mandatory settings, all settings, or a number of additional settings), and the "maximum interleaver delay" in milliseconds. *Id.*at § 12.4.6.1; § 12.4.6.2.1.1.

124. After receiving O-MSG2, the VTU-R sends a message called R-CONTRACT1, which contains "the proposed downstream contract based on the maximal number of bits in the slow channel based on the restrictions specified in O-MSG2 (i.e., as if only the slow channel will be used)." *Id.* at § 12.4.6.3.1.2. The proposed downstream contract specifies, among other things, the bit rate for the slow channel (a multiple of 64 kbit/s), the Reed-Solomon settings for the slow channel (i.e., the codeword length and number of redundancy bytes), and the interleaver setting (i.e., the interleaver depth and block length). *Id.* at § 12.4.6.3.1.2; § 12.4.6.2.1.2.

125. After receiving R-CONTRACT1, the VTU-O sends a message called O-CONTRACTn, which contains a proposed upstream and downstream contract that is based on the capabilities of the VTU-O and VTU-R. G.993.1 at § 12.4.6.2.1.2. The downstream portion of the contract is based on the information provided by the VTU-R in R-CONTRACT1 and,

ideally, is the same as the contract the VTU-R proposed in R-CONTRACT1. *Id.* Both the upstream and downstream portions of the proposed contract include, among other things, the bit rate for the slow channel (a multiple of 64 kbit/s), the Reed-Solomon settings for the slow channel (i.e., the codeword length and number of redundancy bytes), and the interleaver setting (i.e., the interleaver depth and block length). *Id.*

G. <u>The Family 3 Patents</u>

126. The Family 3 patents claim the benefit of U.S. provisional application No. 60/618,269, filed on October 12, 2004. They share a common written description and have the same drawings. Therefore, my references herein will be to the ’882 patent.

127. The asserted claims of the Family 3 patents are generally directed to methods, systems, and apparatuses for allocating shared memory between transmitter and/or receiver latency paths. ’882 patent at col. 4:1-3. The transmitter and receiver latency paths can share an interleaver/deinterleaver memory, which can be allocated to the transmitter’s interleaver and to the receiver’s deinterleaver. *Id.* at col. 4:5-9; col. 9:18-21. The allocation of the shared memory can be based on the data rate, latency, bit error ratio (BER), impulse noise protection requirements, or “any parameter associated with the communications system.” *Id.* at col. 4:9-13; *see also id.* at col. 5:22-27. FIG. 1 of the Family 3 patents, copied below, illustrates, among other things, a transceiver with two latency paths in the transmit direction (210, 220), each including an interleaver (216, 226); two latency paths in the receive direction (310, 320), each including a deinterleaver (316, 326); and a shared memory (120). *Id.* at col. 4:41-56. The shared memory can be allocated to an interleaver and deinterleaver (*id.* at col. 5:33-39), to multiple interleavers in the transmitter (*id.* at col. 5:40-46), or to multiple deinterleavers in the receiver (*id.* at col. 5:47-53).

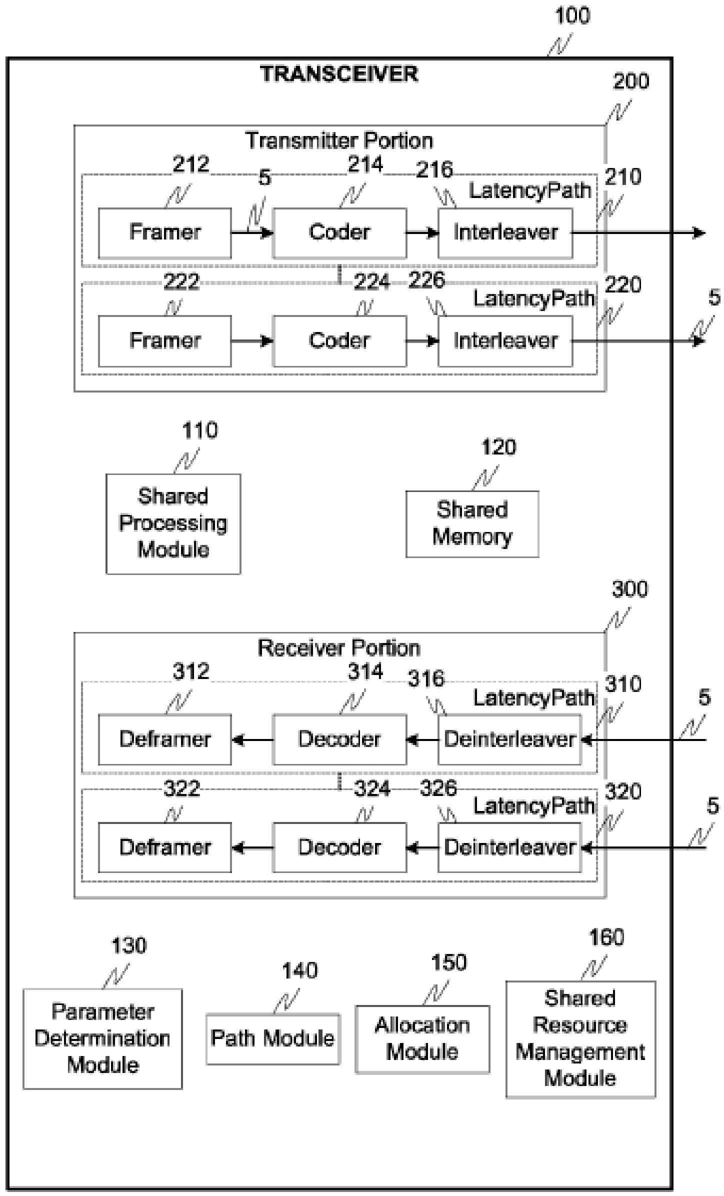


Fig. 1

128. Based on parameters such as data rate, impulse noise protection, bit error rate, or latency, the allocation module 150 allocates a portion of the shared memory 120 to the interleaver(s) and/or deinterleaver(s) in each of the latency paths. *Id.* at col. 5:62-6:3. After determining the memory allocation for each of the latency paths, "the transceiver 100 transmits to a second transceiver one or more of the number of latency paths (N), the maximum interleaver memory for any one or more of the latency paths and/or the maximum total and/or shared memory for all of the latency paths." *Id.* at col. 6:4-11.

129. The Family 3 patents also disclose transmitting framing, coding, and interleaving information from one transceiver to another during initialization or thereafter. *Id.* at col. 7:50-59. In one embodiment, a first modem determines framing, coding, and interleaving parameters to meet application requirements such as latency, burst error correction capability, etc. *Id.* at col. 7:60-63. To do so, "the first modem must know what are the capabilities of a second modem." *Id.* at col. 64-66. Specifically, "the first modem must know" (1) how many latency paths the second modem can support, (2) the maximum amount of interleaver memory for each transmitter latency path, and (3) the total shared memory for all transmitter latency paths. *Id.* at col. 7:66-8:5. The first modem uses this information to "choose a configuration that can meet application requirements and also meet the transmitter portion latency path capabilities of the second modem." *Id.* at col. 8:5-8.

130. The Family 3 patents provide an example in which a first transceiver sends a message to a second transceiver indicating the number of supported transmitter and receiver latency paths, the maximum interleaver memory for each of the latency paths, and the maximum total or shared memory for all of the latency paths. *Id.* at col. 8:9-19. The first transceiver then selects settings (i.e., Reed-Solomon parameter values N and R, and the interleaver depth, D) for each of the latency paths. *Id.* at col. 8:21-22.

131. FIG. 3 of the Family 3 patents, copied below, shows a method of exchanging shared resource allocations.

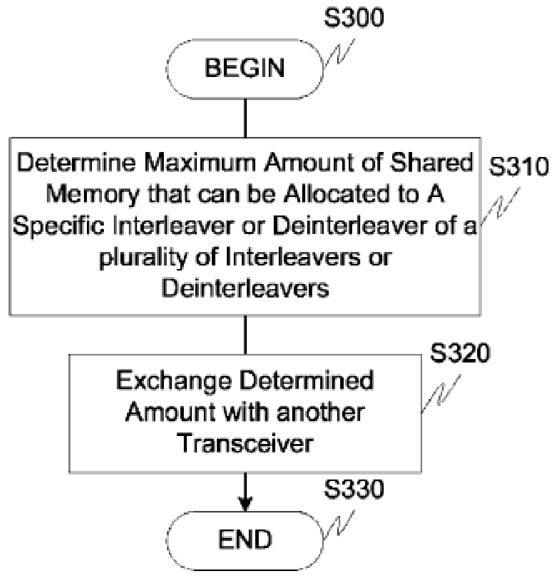


Fig. 3

At step S310, the "maximum amount of shared memory that can be allocated to a specific interleaver or deinterleaver of a plurality of interleavers and deinterleavers in a transceiver is determined." *Id.* at col. 8:62-66. The determined maximum amount for one or more interleavers/deinterleavers is then transmitted to another transceiver in step S320. *Id.* at col. 8:66-9:1. The transceiver can also transmit and/or receive "messages containing additional information," although the Family 3 patents do not provide any examples of such "additional information." *Id.* at col. 9:1-3.

1. <u>Asserted Claims Family 3 Patents</u>

132. The asserted claims of the Family 3 patents are claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent. For convenience, I have given each of the claim elements an identifier, which I use through the rest of this report.

133. Claim 1 of the '048 patent recites:

1[a]. A system that allocates shared memory comprising:

[b] a transceiver that is capable of:

> [c] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;
>
> [d] determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;
>
> [e] allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,
>
> [f] wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;
>
> [g] allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and
>
> [h] interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver,
>
> [i] wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

As corrected by the certificate of correction[5] issued on February 8, 2011, claim 5 of the '381 patent recites:

> 5[a]. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:
>
> [b] transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;

[5] As more particularly described below, following the issuance of both the '381 and '882 patents, the applicant requested and received Certificates of Correction pursuant to 35 U.S.C. § 235 as a result of typographical errors introduced by the applicant related to three limitations included in claims 5 and 13 of those patents, respectively. I have indicated the changes effected by the Certificates of Correction by using strike-through of the language as it appeared originally in the claims, and brackets for the language as corrected.

> [c] determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
>
> [d] allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,
>
> [e] wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;
>
> [f] allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and
>
> [g] deinterleaving the first plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver,
>
> [h] wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

As corrected by the certificate of correction issued on May 3, 2011, claim 13 of the ’882 patent recites:

> 13[a]. A system that allocates shared memory comprising:
>
> [b] a transceiver that performs:
>
> [c] transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;
>
> [d] determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;
>
> [e] allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,

> [f] wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;
>
> [g] allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and
>
> [h] deinterleaving the first plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver,
>
> [i] wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

Claim 19 of the '473 patent recites:

> 19[a]. An apparatus comprising:
>
> [b] a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path,
>
> [c] the multicarrier communications transceiver being associated with a memory,
>
> [d] wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver and
>
> [e] wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

2. <u>Provisional Application</u>

134. I reviewed the provisional application of which the Family 3 patents claim the benefit, namely U.S. provisional application No. 60/618,269 ("the '269 provisional"), filed on October 12, 2004, to determine whether the asserted claims are entitled to a priority date of October 12, 2004. I concluded that they are not.

135. Claim 5 of the ’381 patent, claim 13 of the ’882 patent, and claim 1 of the ’048 patent all require shared memory, “wherein the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver].” I do not see any disclosure of this element in the ’269 provisional, and therefore, in my opinion, claim 5 of the ’381 patent, claim 13 of the ’882 patent, and claim 1 of the ’048 patent are not entitled to a priority date of October 12, 2004.

136. Claim 19 of the ’473 patent requires that “the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.” I do not see any disclosure of this element in the ’269 provisional. The ’269 provisional discloses a receiver deciding how a transmitter will split interleaving memory between multiple interleavers (but not deinterleavers) and states that “an essential aspect of this invention [is] that prior to configuring the FCI blocks the transmitting modem must send a message to the receiving modem containing **information describing the total/shared memory of the <u>transmit</u> FCI blocks**.” ’269 provisional at 5 (emphasis added). As an alternative approach, the ’269 provisional describes the receiving modem sending a message to the transmitting modem to allow the transmitter to determine the transmit FCI configuration, in which case “it is an essential aspect of this invention that prior to configuring the FCI blocks the receiving modem must send a message to the transmitting modem containing **information describing the total/shared memory of the <u>receive</u> FCI blocks**.” ’269 provisional at 5 (emphasis added). When it describes a transceiver sharing interleaver memory “between the transmitting and receiving portions of a single modem,” however, the ’269 provisional does not disclose the transceiver performing any allocation of memory between an interleaving function and a deinterleaving function in accordance with a message received

during an initialization of the transceiver. '269 provisional at 5. Therefore, in my opinion, claim 19 of the '473 patent is not entitled to a priority date of October 12, 2004.

3. File History

137. The Family 3 patents claim priority to Provisional Application No. 60/618,629, filed on October 12, 2004. The applicant filed Utility Application No. 11/246,163 on October 11, 2005, which would eventually issue as the '890 patent, the first of the Family 3 patents. The application for the '890 patent originally included 45 claims, of which claims 37-42 are representative:

> 37. An information storage media having stored thereon information that when executed allows sharing of resources in a transceiver comprising:
>
> information that allocates a first portion of shared memory to a first latency path and information that allocates a second portion of the shared memory to a second latency path.
>
> 38. The media of claim 37, wherein the first latency path includes an interleaver and the second latency path includes an interleaver.
>
> 39. The media of claim 37, wherein the first latency path includes a interleaver and the second latency path includes a deinterleaver.
>
> 40. The media of claim 37, wherein the first latency path includes a deinterleaver and the second latency path includes a deinterleaver
>
> 41. The media of claim 37, further comprising information that transmits to another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.
>
> 42. The media of claim 37, further comprising information that receives from another transceiver information that is used to determine a maximum amount of shared memory that can be allocated.

Application No. 11/246,163, at 28 (Oct. 11, 2005).

138. The Examiner rejected all 45 original claims, including claims 37-42, under 35 U.S.C. 102(e) as being anticipated by Fadavi-Ardekani (U.S. Patent No. 6,707,822). *See* 2/24/2009 Office Action. The applicant attempted to argue that Fadavi-Ardekani was not enabling and not anticipatory (*see* 8/21/2009 Remarks, at 8), but the Examiner rejected those arguments and maintained the rejection of all 45 claims as anticipated by Fadavi-Ardekani. *See* 12/9/2009 Office Action, at pp. 4, 14-15.

139. The Examiner found, for example, that Fadavi-Ardekani teaches methods and systems for "sharing resources in a transceiver" comprising "allocating a first portion of shared memory to a first latency path (i.e., 16 Kbytes is allocated for interleave, lines 25-30 in column 7) and allocating a second portion of the shared memory to a second latency path (i.e., 4 Kbytes is allocated for deinterleave, lines 25-30 in column 7)." *Id*. at 14, 16, 18-19. The Examiner also found that Fadavi-Ardekani teaches transmitting or receiving "information that is used to determine a maximum amount of shared memory that can be allocated." *Id*. at 15, 20. Finally, the Examiner found that Fadavi-Ardekani also teaches that the first latency path may include an interleaver and the second latency path may include either a second interleaver or a deinterleaver. *Id*. at 16, 19.

140. The Examiner and applicant then held an interview, and in an interview summary, the Examiner indicated that "[t]he examiner and applicant discussed an overview of the invention and explained features of simultaneous transfer and types of interleaving and allocation of memory based on direction of transmission and bandwidth." 12/16/2009 Examiner Interview Summary, at 4. The examiner suggested that the Applicant provide more details "such as type of memory, type of interleaving to distinguish from the prior art or memory art." *Id.*

141. Thereafter, the applicant cancelled all 45 claims and introduced new claims 46-53, which the applicant stated "more particularly claim[] certain aspects of the invention," including "a deinterleaver embodiment" reflected by independent claim 50. *See* 12/17/2009 Amendment and Response, at 4; 12/30/2009 Amendment and Response, at 5. The applicant then made one more amendment to both of the newly added independent claims 46 and 50 in order to "correct a typographical error," which was directed to the use of the word "of" in new independent claims 46 and 50. 3/8/2010 Supplemental Amendment and Response, at 2, 3, 5.

142. The Examiner then issued a notice of allowance, which included an "Examiner's Amendment." The Examiner's Amendment indicated that "authorization for this examiner's amendment was given in a telephone interviews with Jason Vick (Reg. No. 45,285) on August 2 and 3, 2010," and that "[s]hould the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312." *See* 9/7/2010 Notice of Allowance, at 2-4. With respect to claim 50, the examiner noted it "identifies the distinct features of specifying a maximum number of bytes available to be allocated to a deinterleaver in a transmitted or received message, determining the amount of memory required to the deinterleaver wherein the bytes allocated do not exceed the maximum number of available bytes specified in the message." *Id.* at 5. The Examiner stated that "the closest prior art, Fadavi-Aredekani . . . discloses sharing a memory between the interleavers and deinterleavers of multiple ADSL sessions, [but] fails to suggest limiting the memory allocated to the deinterleaver to a maximum number of bytes available that was specified in a transmitted or received messages." *Id.*

143. After receiving the notice of allowance, on October 4, 2010, the applicant submitted comments on the Examiner's stated reasons for allowance. The applicant stated that

"[w]hile the stated Reasons for Allowance may be a stated reason for allowing some independent claims, Applicant submits that some independent claims have a different reason for allowance and that some independent claims have other reasons for allowance. Specifically, the prior art fails to teach the specific combination of features as recited in the independent claims 46 and 50." The applicant did not identify any error in the claims or contend that the allowed claims were defective. *See, e.g.*, 10/4/2010 Comments on Statement of Reasons for Allowance, at 1-2 (Application No. 11/246,163).

144. The applicant filed on April 16, 2010, August 9, 2010, and October 11, 2010 the three applications that matured into the '882 patent, the '381 patent, and the '048 patent, respectively. The '381 patent issued on November 16, 2010, and the '882 patent issued on November 30, 2010. The '048 patent did not issue until September 12, 2012.

145. On January 5, 2011, the applicant filed three requests for certificates of correction pursuant to 37 C.F.R. §§ 1.322 and 1.323 for claim 5 of the '890 patent, claim 13 of the '882 patent, and claim 5 of the '381 patent. The applicant stated that the corrections to the '890 patent were necessary due to "mistake[s] of both the Office and the Applicant," specifically, the use of the words "transmission" and "received" in conjunction with the deinterleaving and interleaving functions of the transceiver, rather than "reception" and "transmitted." *See*, *e.g.*, 1/5/2011 Request for Certificate of Correction of Patent for Office's Mistake (37 C.F.R. § 1.322) and Applicant's Mistake (37 C.F.R. § 1.323), at 1 (Application No. 11/246,163). A third word used in the claims, "shred," also was corrected to be recited as "shared." *See id.*

146. The requests for Certificates of Correction in the '882 and '381 patents also sought to correct "shred" and the use of the words "transmission" and "received" in connection

with, respectively, the deinterleaving and interleaving functions of the transceiver. The applicant admitted that the errors in the '882 and '381 patents were due only to mistakes of the applicant. *See, e.g.*, 1/5/2011 Request for Certificate of Correction of Patent for Applicant's Mistake (37 C.F.R. § 1.323), at 1 ('882 patent file history); 1/5/2011 Request for Certificate of Correction of Patent for Applicant's Mistake (37 C.F.R. § 1.323), at 1 ('381 patent file history).

147. Claim 5 of the '048 patent included the same use of the words "transmission," "received," and "shred" that had been the subject of Certificates of Correction for the '890 and '381 patents. In an initial office action dated January 6, 2012 rejecting all the claims, the examiner specifically called attention to the use of "shred," and objected to the claim due to that error. 1/6/2012 Non-Final Rejection, at 2. The examiner did not identify any other errors in the claim language, and in responding to rejection, the applicant did not suggest there were any. *See* 8/3/2012 Amendment and Response, at 6-7.

148. The examiner thereafter issued a Notice of Allowance, once again stating that "[t]he prior arts of record . . . fail to teach, singly or in combination, the claimed invention as whole, especially *transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver*. Notice of Allowance, at 4 (emphasis in original); *see also id.* at 5.

4. <u>Claim Construction</u>

149. I have reviewed the Court's Claim Construction Order for the Family 3 Patents, issued on December 28, 2017. A summary of the terms in the claims of the '882 patent, the '381 patent, the '048 patent, and the '473 patent for which the Court provided a construction is provided below:

Term or Phrase	Court's Construction
"transceiver"	"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry"
"shared memory"	"common memory used by at least two functions, where a portion of the memory can be used by either one of the functions"
"amount of memory"	plain meaning
"the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]	"the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"
"latency path"	"transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay"
"wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message"	plain meaning
"portion of memory"	plain meaning
"memory is allocated between the [first] interleaving function and the [second interleaving / deinterleaving] function"	"an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"

150. In my analysis, I have applied the Court's constructions. I have interpreted the remaining claim terms as they would have been understood by a person having ordinary skill in the art on the priority date of the Family 3 patents, considering the context of the claims themselves, the specification, the figures, the prior art, and the prosecution history. Consistent with these constructions and interpretations, I have considered the claims in light of the ordinary meaning of the claims based on the perspective of one of skill in the art and consistent with my experience in the field.

VIII. ANALYSIS OF INVALIDITY UNDER 35 U.S.C. § 112

A. 35 U.S.C. § 112, ¶ 2 – Indefiniteness

151. It is my opinion that claim 19 of the '473 patent is indefinite. Claim 19 recites the limitation "wherein at least a portion of the memory ***may be*** allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." One of ordinary skill in the art would not have known with reasonable certainty whether a portion of the memory actually has to be allocated to an interleaving function at one time, and a deinterleaving function at another, or whether the mere possibility that some portion of the memory could possibly be allocated to the interleaving or deinterleaving function suffices to meet the claim language. I note that the Court determined that this language should have its plain meaning during claim construction.

152. The use of the permissive language "may be allocated" makes it impossible for a skilled artisan to determine with reasonable certainty whether the claim is infringed, because it is not clear, when reading the claims, specification, and file history, whether the memory actually has to be allocated in more than one way. Given the '473 patent's disclosure, one of ordinary skill in the art would have understood that, within the shared memory, a particular memory space may be allocated to the interleaver or the deinterleaver depending on the current demands of the system, and in turn, a message. It is not clear from the intrinsic record, however, whether this allocation actually has to happen, at some point, in order for a device to infringe. For example, a system could use a shared memory in such a way that it is theoretically possible that a portion of the memory is allocated to a deinterleaver or an interleaver, depending on the message, but it might not actually ever happen in practice. One of ordinary skill in the art would not have understood whether such a system would infringe claim 19 of the '473 patent.

B. 35 U.S.C. § 112, ¶ 1 – Written Description and Enablement

153. It is my opinion that the term "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]" in claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent lacks written description and enablement. I note that the Court construed this term to mean "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." The specification, claims, and file history do not demonstrate to one of ordinary skill in the art that the inventors had possession of the claimed invention as of the filing date in accordance with the Court's construction.

154. The specification describes sharing resources, such as memory and processing power, as well as ways of allocating those shared resources. It does not, however, describe or explain how shared memory that is allocated to an interleaver and a deinterleaver can be used at the same time, or even what "used at the same time" even means. Notably, the phrase "used at the same time" does not appear in the written description. One of ordinary skill in the art would not have understood that the inventor was in possession of this aspect of the invention when the application was filed.

155. It is also my opinion that the claim term "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message" in claim 19 of the '473 patent lacks written description. I understand that the Court determined that this term should have its plain meaning.

156. One of ordinary skill in the art would not have understood the patentee to have been in possession of an apparatus wherein at least a portion of the memory may be allocated to a first interleaving function or a second interleaving function at any one particular time depending on the message. The specification describes ways of allocating shared memory between an interleaving function and a deinterleaving function, but it does not describe to one of ordinary skill in the art how at least a particular portion of the memory can be allocated to one function, and then be allocated to the other function at any one particular time.

C. Certificates of Correction

157. I was asked to opine on whether a person having ordinary skill in the art would have recognized certain terms in claim 5 of the '381 patent and claim 13 of the '882 patent, as they originally issued, to be "typographic errors" such that the changes made to these terms in the Certificate of Correction did "not materially affect the scope or meaning of the patent" as the applicant represented to the Patent Office in its requests for Certificates of Correction.

158. I believe that a person having ordinary skill in the art would have understood the word "shred" in the issued patents to be an obvious typographical error, particularly because it is followed by the word "memory," and the claims recite "shared memory" elsewhere.

159. I do not, however, believe that a person having ordinary skill in the art would have considered the terms "transmission" and "received" in claim 5 of the '381 patent and claim 13 of the '882 patent to be typographical errors. For example, as issued, both claims recited "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. . ." and "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate." As a skilled artisan would have understood, there is no reason why a

transceiver could not deinterleave a first plurality of Reed-Solomon coded data bytes and then transmit them at a first data rate, nor is there any reason why a transceiver could not receive a second plurality of Reed-Solomon coded data bytes at a second data rate and then interleave them. The Family 3 patents do not appear to foreclose either of these possibilities. Indeed, the Family 3 patents state that "it should be appreciated that this invention can be applied to any transceiver having any number of latency paths," which a person having ordinary skill would have understood to include transceivers that allocate "a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate" and "a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received at a second data rate."

160. Moreover, in my opinion, a person having ordinary skill in the art would have considered the changes made by the Certificates of Correction to materially affect the scope and meaning of the issued patents. A skilled artisan would have understood transmission and reception to be different, and that requiring transmission instead of reception, or vice versa, changes the required functionalities of the claimed transceivers. A skilled artisan would also have understood that a transceiver that did not infringe claim 5 of the '381 patent or claim 13 of the '882 patent as issued could infringe claim 5 of the '381 patent and claim 13 of the '882 patent as modified by the Certificates of Correction. In my opinion, this fact means that the changes made through the Certificates of Correction changed the scope and meaning of the '381 and '882 patents.

IX. ANALYSIS OF THE PRIOR ART

161. It is my opinion that each of the asserted claims of the Family 3 patents are rendered obvious by prior art as I describe below. In my analysis below, I opine on the claim language as corrected by the certificates of corrections filed by the applicant.

A. The Asserted Claims Are Obvious Over LB-031

162. ITU-T SG/15/Q4 Contribution LB-031 ("LB-031"), entitled "VDSL2 – Constraining the Interleaver Complexity," was a contribution to the June 14-18, 2004 meeting of SG15/Q4, held in Leuven, Belgium. The first page of LB-031 indicates that it was a revision of a T1E1.4 contribution made in 2003 and numbered T1E1.4/2003-493.

163. It is my opinion that claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent are rendered obvious by LB-031 in view of the knowledge of one of ordinary skill in the art. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then LB-031 renders obvious the asserted claims of the Family 3 patents.

1. Public Availability of LB-031

164. LB-031 was made available to SG15/Q4 electronically via the SG15/Q4 document server at least by June 16, 2004.[6] Per the SG15/Q4 operating rules, it should have been uploaded to the document server by at least June 7, 2004. *See, e.g.*, LB-004 ("Contributions for the ITU Rapporteur meeting should be uploaded to the ftp site one week prior to the start of the Rapporteur meeting. Generally, for a Monday Rapporteur meeting start,

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[6] *See* 00_doc_list.html, which was generated on June 16, 2004 by Steve Palm, one of the Associate Rapporteurs of SG15/Q4, and includes a link for LB-031; *see also* LB-000.txt, which lists the contributions to the Leuven meeting, including LB-031.

papers should be submitted by end of day on the prior Monday. Before presentation of a contribution, the electronic version of the paper shall be provided to the Rapporteur."). Once uploaded to the document server, LB-031 would have been available to SG15/Q4 participants world-wide. *See, e.g.*, LB-004 ("The use of electronic document submission and distribution is a key factor in improving the efficiency of Q4/SG15 operation. The guidelines below will insure that all meeting attendees have advance capability to review contributions presented for Rapporteur meetings. The basic principals [sic] are that documents are posted on the ITU informal WEB site and access to the WEB is available world wide.").

165. The VDSL issues list, used by SG15/Q4 to track work item status, open questions, and agreements, indicates that LB-031 was presented and discussed at the Leuven meeting, and three new open issues were added to the VDSL issues list based on the content and discussion of LB-031. *See* LB-U11R4, item 11.4 (adding questions "Should interleaver complexity be specified in terms of a time delay (ms), not in terms of an amount of memory or an interleaver depth?" and "Should interleaver delay in terms of octets be exchanged between the VTU-O and VTU-R; Should the delay in octets meet the minimum requirements in terms of the delay in time?" and "Should the upper limit on the number of codewords per unit time be constrained and scale with the data rate so that as the data rates increase, this upper limit on the number of codewords is also higher?"); *compare* LB-U11, item 11.4 (VDSL2 issues list at beginning of Leuven meeting did not include questions quoted above). Marcos Tzannes, a named inventor on the Family 3 patents, submitted contributions to the Leuven meeting. *See* 00_doc_list.html, LB-000.txt. I also encountered Mr. Tzannes at a number of other SG15/Q4 meetings that I attended. Mr. Tzannes served as Associate Rapporteur for the G.bond and G.test projects of SG15/Q4.

2. Brief Description of LB-031

166. LB-031 proposes to set particular restrictions on the interleaver to be specified for the VDSL2 standard being developed by SG15/Q4. LB-031 at 1. LB-031 begins with a tutorial on convolutional interleaving and derives equations to illustrate trade-offs between interleaver memory size, error correction capability, delay, and error burst separation. Denoting the block size as *I* and the interleaver depth as *d*, LB-031 explains that the end-to-end delay of the interleaver/deinterleaver pair, in octets (i.e., bytes) is given by

$$\text{interleaver delay} = (I - 1) \times (d - 1) \text{ octets} \qquad \text{(Eq. 1)}$$

and that "[t]the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver." *Id.* at 2. LB-031 teaches that the amount of memory used to implement the interleaver is typically approximately the same as the amount of memory used to implement the deinterleaver, and that the smallest possible amount of memory for either is given by:

$$\text{smallest possible (de)interleaver memory} = (I - 1) \times (d - 1)/2 \text{ bytes} \qquad \text{(Eq. 2)}$$

Id. LB-031 explains that "[i]n a typical implementation, slightly more memory is often required," and "[t]he actual amount of required memory is implementation specific." *Id.*

167. LB-031 teaches that "[t]he length of a burst that can be corrected by the combination of Reed-Solomon coding and interleaving/deinterleaving is dependent on the line data rate," denoted in LB-031 as *ldr*, which is the bit rate of the Reed-Solomon encoded bits. *Id.* The line data rate *ldr* is higher than the net data rate, denoted as *ndr*, which is the user data rate. *Id.* LB-031 uses the notation *ldr_mbit_s* to indicate when the line data rate is in Mbit/s and *ldr_kbit_s* to indicate when the line data rate is in kbit/s. Denoting the Reed-Solomon codeword length as *n* and the number of Reed-Solomon redundancy bytes as *r*, LB-031 teaches that the line data rate and net data rate are related by the equation

$$ndr\_kbit\_s = ldr\_kbit\_s \times (n - r)/n - \text{overhead rate} \qquad \text{(Eq. 3)}$$

Id. As a person having ordinary skill in the art would have recognized as of the Family 3 patents' priority date, the "overhead rate" would include any additional bit rate consumed for the transmission of bits that do not convey user data (e.g., cyclic redundancy check bytes, messages transmitted to the far-end transceiver for operations, administration, and maintenance purposes, etc.).

168. LB-031 notes that the Reed-Solomon code can correct t bytes in error, where $t = r/2$. *Id.* It also explains that the Reed-Solomon codeword size n can be an integer multiple of the interleaver block size I, i.e., $n = I \times q$. *Id.* Consequently, the combination of Reed-Solomon coding and interleaving can correct a burst of errors up to $t \times d/q$ octets long. *Id.* By accounting for the line data rate, the maximum duration of a burst of errors that can be corrected can be determined. Converting to time, the duration of a burst of errors can be up to

$$\text{INP\_min} = t \times \frac{d}{q} \times \frac{8}{ldr\_mbit\_s}\ \mu\text{s} \qquad \text{(Eq. 4)}$$

In equation 4, "INP_min" denotes the impulse noise correction, and the "8" in the numerator is the number of bits per byte to make the units of the quantity microseconds. *Id.* at 2, 5.

169. LB-031 provides an example using the equations for ADSL2 and ADSL2+, in which $q = 1$ (i.e., the interleaver block size is equal to the Reed-Solomon codeword length), the maximum value of t is 8 (corresponding to 16 redundancy bytes), the maximum value of the Reed-Solomon codeword length n is 255, and the maximum value of the interleaver depth d is 64 in the downstream direction and 8 in the upstream direction. *Id.* at 2. Assuming the maximum line data rate of 24.48 Mbit/s in ADSL2+, the use of Reed-Solomon coding plus interleaving can correct a burst of errors up to $8 \times 64/1 \times 8/24.48 = 167$ µs in duration. *Id.*

170. LB-031 notes that the end-to-end interleaver delay, in milliseconds, is

$$(I - 1) \times (d - 1) \times 8/ldr\_kbit\_s \text{ (Eq. 5)}$$

Id. For the maximum line data rate and largest values of I and d in ADSL2+, the delay is $(255 - 1) \times (64 - 1) \times 8/24480 = 5.23$ ms.

171. LB-031 teaches that "[e]rror bursts must be separated in time so that each codeword corrects only one burst." *Id.* The span (i.e., time over which a single codeword extends after interleaving) of a Reed-Solomon codeword of size n octets (bytes) and an interleaver depth of d is equal to

$$n \times d/q \times 8/ldr\_kbit\_s \qquad \text{(Eq. 6)}$$

Id. Because $n = I \times q$, the span is nearly identical to the end-to-end interleaver delay given in Equation 5 for large codeword size n and depth d. *Id.* Using the ADSL2+ example from above, at the maximum codeword size, interleaver depth, and line data rate, each codeword spans $(255) \times (64) \times 8/24480 = 5.33$ ms. *Id.* at 3. Thus, in ADSL2+, at the maximum line data rate and codeword size, the combination of coding and interleaving can correct a burst of duration 167 µs every 5.33 ms. *Id.*

172. LB-031 observes that "[m]ore interleaver memory normally allows more error correction but leads to higher delays and a longer separation between error bursts." *Id.* Although "[s]ignificant error correction can be achieved by using shorter codewords requiring less memory, less delay, and shorter time between bursts," shorter codewords "typically have lower net coding gain and higher computation requirements since there are more decoder operations required in the same amount of time." *Id.* Thus, there is a trade-off between complexity, capability, and performance. *Id.*

173. LB-031 observes that "[t]he size of the interleaver memory will be a major source of complexity in VDSL2." *Id.* ADSL2 specifies the smallest maximum interleaver

depth and the maximum number of Reed-Solomon codewords in a DMT symbol. *Id.* LB-031 points out two problems with adopting the same approach for VDSL2: (1) "it removes the flexibility of trading codeword size and interleaver depth to allow more error correction with the same amount of memory," and (2) as the data rate increases, the end-to-end interleaver delay decreases, which leads to less error correction capability. *Id.*

174. Because the VDSL2 data rate requirements of different service providers extend over a large range, LB-031 suggests defining "the interleaver complexity requirements in a way that will allow those who want to deploy VDSL2 at lower speeds to do so at a reduced complexity with respect to higher speed implementations." *Id.* Because the end-to-end interleaver delay in units of time is proportional to the interleaver depth and inversely proportional to the line data rate, as shown in Equation 5, LB-031 proposes to specify the interleaver complexity in terms of the end-to-end interleaver delay in units of time. *Id.* LB-031 suggests that requiring VDSL2 interleavers to support a delay of at least 5.23 ms (the value that results when ADSL2+ operates at the maximum line data rate, maximum interleaver delay, and maximum codeword size). *Id.*

175. LB-031 teaches:

> For interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate. If a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value. The VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.

Id. LB-031 emphasizes again that "the actual amount of memory required is implementation specific." *Id.*

176. As an example of the proposed approach, LB-031 uses Equations 1 and 5 to determine the minimum memory size required in each of the interleaver and deinterleaver for a VDSL2 line data rate of 44.5 Mbit/s and a minimum interleaver delay requirement of 5.23 ms. *Id.* at 4. From Equation 5, the value of $(I-1) \times (d-1)$ is 29092 bytes, and from Equation 1, the end-to-end delay of the interleaver in octets (bytes) is then also 29092. From Equation 2, the interleaver would need to have "*at least* 14546 octets" (bytes), although the amount actually used would be implementation-specific. *Id.* (emphasis in original). The VDSL2 transceiver would indicate, during the initialization procedure, that it can support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay. *Id.* LB-031 notes that if the line data rate ends up being much less than 44.5 Mbit/s, the delay using the entirety of the interleaver memory could be quite large, and "[t]his is why the maximum delay is still needed." *Id.*

177. LB-031 proposes that SG15/Q4 agree that "interleaver complexity should be specified in terms of a time delay (ms), not in terms of an amount of memory or an interleaver depth," and "interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R; the delay in octets should meet the minimum requirements in terms of the delay in time." *Id.* at 6.

3. <u>Claim 1 of the '048 Patent</u>

178. It is my opinion that claim 1 of the '048 patent is obvious over LB-031 in view of the knowledge of one of ordinary skill in the art at the time of the alleged invention.

a. <u>1[a]. "A system that allocates shared memory"</u>

179. It is my opinion that a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood LB-031 to disclose the preamble, limitation 1[a] of claim 1 of the '048 patent, to the extent that it is limiting. *See, e.g.*, LB-031 at p. 3.

180. LB-031 discloses allocating memory between an interleaver and a deinterleaver in a VDSL system. LB-031 identifies as an issue "tradeoffs between interleaver memory, error correction capability, delay, and burst separation." *Id.* at p. 3. It then proposes that "the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate." *Id.* LB-031 goes on to provide an example of allocating memory between an interleaver and a deinterleaver, in which "[i]f the minimum interleaver delay requirement were 5.23 ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of *at least* 14546 octets according to equation (2)." *Id.* at 4 (emphasis in original). One of ordinary skill in the art on the priority date of the Family 3 patents would have understood this example to teach allocating memory for interleaving and deinterleaving.

181. In my opinion, one of ordinary skill in the art would have understood from the disclosures of LB-031 that the allocated memory can be a shared memory. I note that the Court construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." LB-031 describes how "[t]he size of the interleaver memory will be a major source of complexity in VDSL2." *Id.* at 3. It further explains how VDSL2 has stated 100 Mbit/s as a stated goal for data rate, but that "a number of operators have stated their requirements at well below 100 Mbit/s." *Id.* LB-031 further explains that the actual amount of memory required for interleaving and deinterleaving is implementation specific, and that a VDSL2 implementation can support a larger memory than is actually required. *Id.*

182. As I explained above in Section VII.C, it was well known by the priority date of the Family 3 patents that an interleaver and deinterleaver could share a memory, including in DSL implementations. *See, e.g.*, U.S. Patent Pub. No. 2005/0034046 by Berkmann *et al.* at Abstract (disclosing a "combined interleaving and deinterleaving circuit" with "data memory (RAM) for temporary storage of the data to be interleaved and deinterleaved"); U.S. Patent No. 6,707,822 to Fadavi-Ardekani *et al.* at Abstract (disclosing an "Interleave/De-Interleave Memory" that "is shared by multiple ADSL sessions and by the transmit and receive processes within an individual session"); U.S. Patent No. 6,381,728 to Kang at col. 5:35-38 (disclosing "double buffering [that] allows the channel interleaver memory to be used, along with the app memory, as the turbo deinterleaver memory"); U.S. Patent No. 7,269,208 to Mazzoni *et al.* at Abstract (disclosing memory having "a first memory space assigned to the interleaver and a second memory space assigned to the deinterleaver" of a VDSL transceiver); U.S. Patent No. 5,751,741 to Voith *et al.* at col. 4:47-50 (disclosing external interleave/deinterleave memory used by both transmitter for interleaving and receiver for deinterleaving).

183. Consequently, a person having ordinary skill in the art as of the Family 3 patents' priority date would understood that, by recognizing the negative effects of complexity and size of interleaver memory, LB-031 discloses the allocation of a "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions" for the interleaver and deinterleaver.

b. <u>1[b]. "a transceiver that is capable of"</u>

184. It is my opinion that LB-031 discloses limitation 1[b]. *See, e.g.*, LB-031, at pp. 3-4.

185. LB-031 describes that "[d]uring initialization, the VDSL2 transceiver would indicate" its capabilities. LB-031 at 4. LB-031 describes the use of a VDSL2 VTU-O and

VTU-R to allocate memory for interleaving and deinterleaving; one of ordinary skill in the art would have understood the VTU-O and VTU-R to be transceivers. *Id.* at 3. LB-031 also provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4.

186. I understand that the Court construed the term "transceiver" to mean "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry." One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031 both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory, in addition to other circuitry, such as, for example, an interface to the twisted pair.

c. 1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"

187. In my opinion, LB-031 discloses limitation 1[c]. *See, e.g.*, LB-031, pp. 3, 6.

188. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. The O-PMS message includes a parameter referred to as "max_delay_octet." *See* G.993.2 (12/2011), § 12.3.5.2.1.3, Table 12-56. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then the message specifying interleaver delay in octets described in LB-031 discloses this limitation under such an interpretation of the claims.

189. LB-031 states that "[d]uring initialization, the VDSL2 transceiver would indicate" its capabilities, and that these capabilities include the maximum bit rate it can support, the maximum supported end-to-end delay in octets, and the maximum delay in ms. LB-031 at

pp. 4, 6. LB-031 also discloses that "[f]or interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets." *Id.* at 3; *see also* 6 ("interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time."). LB-031 states that "[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate," but that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," in which case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities." *Id.* at 3.

190. LB-031 describes the relationship between the interleaver delay in octets and interleaver memory, noting that "the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver" and providing equations that describe that relationship, which I explained above at Section IX.A.2. *Id.* at 2. Thus, the information exchanged during initialization includes the maximum end-to-end interleaver delay in octets, which meets this limitation under TQ Delta's interpretation of the claims.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory"

191. LB-031 discloses limitation 1[d], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4.

192. LB-031 describes, though a series of equations, the amount of delay imposed by a convolutional interleaver/deinterleaver pair, as well as how the "smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver." *Id.* at 2 (equations (1) and (2) describing delay and total memory respectively). LB-031 also describes the relationship between Reed-Solomon coding

parameters and octets, and their respective effects on the end-to-end delay of an interleaver. *Id.* at 2 (equations (4) and (5)). Moreover, LB-031 describes trading codeword size and interleaver depth to achieve a desired level of error correcting capability. *Id.* at 3; *see also id.* at 4 (VDSL2 transceiver determines amount of memory to use for interleaving based on octets of memory available and maximum delay). One of ordinary skill in the art as of the Family 3 patents' priority date would have understood that LB-031 describes the VDSL2 transceivers determining an amount of memory required by an interleaver to interleave to interleave a first plurality of Reed Solomon coded data bytes within a shared memory.

e. <u>1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"</u>

193. It is my opinion that LB-031 discloses limitation 1[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

194. First, LB-031 discloses VDSL2 transceivers, a VTU-O and a VTU-R, which one of ordinary skill in the art would have understood to allocate a first number of bytes of shared memory to an interleaver (i.e., the VTU-O allocates shared memory to the interleaver for downstream transmission, and the VTU-R allocates shared memory to the interleaver for upstream transmission). *See* LB-031, at p. 3. The example at p. 4 of LB-031 indicates that during initialization, a VDSL2 transceiver indicates the maximum data rate and maximum delay it can support. As a person having ordinary skill in the art on the priority date of the Family 3 patents would have understood, based on the actual data rate, the VTU-O and VTU-R transmitters then allocate a first number of bytes of the memory to their interleavers.

195. Second, LB-031 discloses interleaving Reed-Solomon coded data bytes for transmission at a first data rate. For example, LB-031 explains the dependence of end-to-end

delay of the interleaver/deinterleaver pair on line rate, Reed Solomon codeword size, and other parameters. *Id.* at pp. 2-3; *see also id.* at p. 4-5 (discussing enhancing correction capability of Reed-Solomon code by using smaller codewords and larger interleaver depth). LB-031 also discloses that "the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that "for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at LB-031 at p. 2. From these and other disclosures in LB-031, one of ordinary skill in the art would have understood that LB-031 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

f. <u>1[f]. "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message"</u>

196. LB-031 discloses limitation 1[f], in my opinion, under TQ Delta's interpretation of the claims. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

197. I have reviewed TQ Delta's infringement contentions, and I understand that TQ Delta contends that the "maximum number of bytes in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's infringement position. To the extent that the Court or the trier of fact interprets the claim consistently with TQ Delta's contentions, however, LB-031 discloses this limitation in my opinion.

198. As explained above, the example at p. 4 of LB-031 indicates that during initialization, a VDSL2 transceiver indicates the maximum data rate and maximum delay it can support. As a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood, the transceivers would exchange this information for both the

downstream and upstream directions. Based on the actual data rate and a specified maximum delay, each transmitter then allocates a first number of bytes of the memory to its interleaver. As a person having ordinary skill in the art on the Family 3 patents' priority date would have understood, neither transceiver would allocate interleaver memory to itself in a manner inconsistent with a message it transmitted in which it indicated its capabilities. Therefore, LB-031 discloses that the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. *See, e.g.*, LB-031 at p. 4 (example of transceiver indicating support of delay of at least 29092 octets allocating up to 14546 octets to interleaver, which is less than 29092 octets indicated in message).

199. Furthermore, as described above, the equations in LB-031 describe tradeoffs between "interleaver memory, error correction capability, delay, and burst separation." *Id.* at p. 3. LB-031 further specifies that "[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate." *Id.* at p. 3. Given these constraints, LB-031 places limits on data rates, codeword sizes, levels of impulse noise protection to meet the constraints of interleaver delay, and in turn, available interleaver memory. *Id.* at 5 ("This does not mean that n=85 would be the largest or smallest codeword size allowed, it is simply used to guarantee a certain minimum level of impulse noise protection at a given minimum interleaver delay at a given maximum data rate. If the actual interleaver delay is higher or the data rate lower or the impulse noise protection lower, larger codewords can be used."). One of ordinary skill in the art would have understood that because of these tradeoffs between interleaver memory and other parameters, a system according to LB-031 would not allocate more memory for its own interleaver than the maximum memory available according to the message.

200. LB-031 further provides a number of examples where the optimal interleaver or deinterleaver memory size does not exceed the amount of memory required by the delay and other parameters. *See id.* at 6.

g. <u>1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"</u>

201. In my opinion, LB-031 discloses limitation 1[g]. *See, e.g.*, LB-031, pp. 2-3, 5, 6.

202. First, as I explained above, LB-031 discloses that the VTU-O and VTU-R exchange their capabilities regarding maximum data rate and maximum delay during initialization. *See, e.g.*, LB-031 at p. 4. As I also explained above, a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood that the transceivers would exchange this information for both downstream and upstream transmission (i.e., the information exchanged would relate to the VTU-O's interleaver and deinterleaver and the VTU-R's interleaver and deinterleaver). Based on this information, each transmitter then allocates a first number of bytes of its memory to its interleaver and a second number of bytes of its memory to its deinterleaver.

203. Second, as I also explained above, LB-031 discloses interleaving Reed-Solomon coded data bytes for transmission at a first data rate. LB-031 explains that the end-to-end delay of the interleaver/deinterleaver depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* at pp. 2-3; *see also id.* at p. 4-5 (discussing enhancing correction capability of Reed-Solomon code by using smaller codewords and larger interleaver depth). LB-031 also discloses how "the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that "for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at LB-031 at p. 2. From these and other disclosures in LB-031, one of ordinary skill in the art would have

understood that LB-031 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate.

h. <u>1[h]. "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"</u>

204. In my opinion, LB-031 discloses limitation 1[h]. *See, e.g.*, LB-031, p. 3.

205. I described above the process by which LB-031 allocates memory to the interleaver and to the deinterleaver above with respect to those sections. LB-031 also discloses a convolutional interleaver, which would operate to interleave RS coded data bytes at the transmitter. *Id.* at p. 2. As a skilled artisan would have understood, the receiver would include a corresponding convolutional deinterleaver, which would operate to deinterleave RS coded data bytes. Moreover, because LB-031 discloses a VDSL2 VTU-O and a VTU-R, one of ordinary skill in the art would have understood that the VTU-O (or VTU-R) would interleave the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver, and the deinterleaver would deinterleave the second plurality of RS code data bytes within the shared memory allocated to the deinterleaver.

i. <u>1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"</u>

206. It is my opinion that LB-031 discloses limitation 1[i]. *See, e.g.*, LB-031, p. 3.

207. I understand that the Court has construed the term "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]" as "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the

interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." LB-031 discloses interleaving and deinterleaving for VDSL transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits data downstream and receives data upstream at the same time, and the VTU-R transmits data upstream and receives data downstream at the same time). This duplex transmission would require that the deinterleaver be able to read from, write to, or hold information for deinterleaving in the portion of memory allocated to the deinterleaver at the same time the interleaver is able to read from, write to, or hold information for interleaving in the portion of memory allocated to the interleaver. Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.[7]

4. Claim 5 of the '381 Patent

208. It is my opinion that each limitation of claim 5 of the '381 patent is obvious over LB-031 in view the knowledge of one of ordinary skill in the art.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

209. To the extent that this preamble is limiting, it is my opinion that LB-031 discloses this limitation. *See, e.g.*, LB-031, p. 3.

210. LB-031 discloses the use of an interleaver pair in a VDSL2 VTU-O and VTU-R. *See id.* at p. 3. One of ordinary skill in the art would have understood that source code and

[7] As I explain above at Section VIII.B, it is my opinion that this limitation is not enabled and lacks written description. To the extent that this limitation is described and enabled by the intrinsic record of the Family 3 patents, it is rendered obvious by the prior art as I describe here, and elsewhere within my report.

instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code. I discuss how LB-031 discloses allocating shared memory in a transceiver above with respect to claim 1 of the '048 patent, which I incorporate here by reference. *See* Section IX.A.3.a. I describe how LB-031 discloses a transceiver above at Section IX.A.3.b, which I also incorporate by reference. Thus, LB-031 discloses this limitation.

b. <u>5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"</u>

211. In my opinion, LB-031 discloses limitation 5[b]. *See, e.g.*, LB-031, pp. 3, 6.

212. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. The O-PMS message includes a parameter referred to as "max_delay_octet." *See* G.993.2 (12/2011), § 12.3.5.2.1.3, Table 12-56. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then LB-031 discloses this limitation under such an interpretation of the claims.

213. Above at Section IX.A.3.c, I describe how LB-031 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver under TQ Delta's interpretation of the claims, and I incorporate this discussion by reference.

214. LB-031 discloses that during initialization, the VTU-O and VTU-R exchange, among other things, the maximum delay supported, in octets (bytes). As I explained above, LB-031 indicates that the VTU-O and VTU-R exchange this information for both the downstream

and upstream directions of transmission. As a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood, the maximum delay is the end-to-end delay between one transceiver's interleaver and the other transceiver's deinterleaver.

215. Furthermore, LB-031 discloses that "[t]ypically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at 2. One of ordinary skill in the art would have understood that the relationships described in LB-031 between delay, interleaver memory size, data rate and other transmission parameters are for an interleaver or a corresponding deinterleaver. Thus is it my opinion that LB-031 discloses this limitation under TQ Delta's interpretation of the claims.

c. <u>5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"</u>

216. LB-031 discloses limitation 5[c], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4.

217. Above at Section IX.A.3.d, I describe how LB-031 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my opinions by reference. LB-031 discloses the relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. *See id.* at p.3. Accordingly, LB-031 discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleaver a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. <u>5[d] "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"</u>

218. In my opinion, LB-031 discloses limitation 5[d]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

219. Above at Section IX.A.3.e, I explain how LB-031 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In addition, at Section IX.A.3.g above, I explain how LB-031 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of these discussions by reference, and on that basis, it is my opinion that LB-031 discloses this limitation.

e. <u>5[e]. "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"</u>

220. In my opinion, LB-031 discloses limitation 5[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6.

221. I have reviewed TQ Delta's infringement contentions, and I understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's infringement position. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, LB-031 discloses this limitation in my opinion.

222. Above at Section IX.A.3.f, I explain how LB-031 discloses "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message," and I incorporate that discussion by reference. In the same way that the VTU-

O or VTU-R of LB-031 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

f. <u>5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"</u>

223. LB-031 discloses limitation 5[f], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 5, 6.

224. Above at Section IX.A.3.e, I explain how LB-031 allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.A.3.g above, I explain how LB-031 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and on that basis, it is my opinion that LB-031 discloses this limitation.

g. <u>5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"</u>

225. LB-031, in my opinion, discloses limitation 5[g]. *See, e.g.*, LB-031, p. 3, 6.

226. Above at Section IX.A.3.h, I explain how LB-031 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being

interleaved, in my opinion, there is no difference in how a transceiver would implement this limitation. It is my opinion that LB-031 discloses this limitation.

h. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

227. LB-031 discloses limitation 5[h], in my opinion. *See, e.g.*, LB-031, pp. 3, 6.

228. I explain above at Section IX.A.3.i that it is my opinion that LB-031 discloses wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference in these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by LB-031.

5. Claim 13 of the '882 Patent

229. In my opinion, LB-031 discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. "A system that allocates shared memory"

230. To the extent that this preamble is limiting, LB-031 discloses a system that allocates shared memory. *See, e.g.*, LB-031, p. 3. This limitation is identical to the preamble of Claim 1 of the '048 patent, and for the same reasons, it is my opinion that this limitation is disclosed by LB-031. *See* Section IX.A.3.a.

b. 13[b]. "a transceiver that performs"

231. In my opinion, LB-031 discloses limitation 13[b]. *See, e.g.*, p. 3, 4. This limitation is identical to the second limitation of Claim 1 of the '048 patent, except that it recites "a transceiver capable of" additional steps. In my opinion, this limitation is met for the same

reasons that limitation 1[b] of the ’048 patent is met, as I explain above at Section IX.A.3.b, and I incorporate my opinions herein by reference.

c. <u>13[c] through 13[i].</u>

232. Limitations 13[c] through 13[i] of claim 13 of the ’882 patent are substantially identical to limitations 5[b] through 5[h] of claim 5 of the ’381 patent. *See* Appx. 3 (comparing limitations of claim 13 of the ’882 patent to claim 5 of the ’381 patent). I incorporate by reference my opinions with respect to those limitations set forth in Sections IX.A.3.c through IX.A.3.i (claim 1) and IX.A.5.b through IX.a.5.h (claim 5). For the same reasons, it is my opinion that those limitations are met by LB-031.

6. <u>Claim 19 of the ’473 Patent</u>

233. In my opinion, LB-031 discloses each limitation of claim 19 of the ’473 patent.

a. <u>19[a]. “An apparatus comprising”</u>

234. To the extent that this preamble is limiting, LB-031 discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, LB-031, pp. 3, 4.

b. <u>19[b]. “a multicarrier communications transceiver”</u>

It is my opinion that LB-031 discloses limitation 19[b]. *See, e.g.*, LB-031, pp. 3, 4. I understand that the Court has construed the term “transceiver” to mean “communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry.”

235. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have understood to be VDSL2 transceivers. *Id.* at 3. LB-031 further provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4. One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031

both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory in addition to other circuitry, such as, for example, an interface to the twisted pair.

236. LB-031 generally deals with VDSL2, which one of ordinary skill in the art would have understood to be a multicarrier communications system. *See, e.g.*, LB-U11R4, item 1.1 (indicating agreement in January 2004 "to develop a subsequent VDSL2 Recommendation that shall specify only DMT modulation, and shall be based on ITU Rec. G.993.1-2004 (VDSL) and ITU Rec. G.992.3 (ADSL2)."). Moreover, LB-031 describes the use of DMT symbols, which are used in multicarrier communications. *See, e.g.*, LB-031 at p. 4 ("Similar to the interleaver delay, we propose that the maxiumum number of codewords in a DMT symbol (or per unit time) also scale with the data rate. The higher the data rate, the more DMT codewords there can be in a fixed length DMT symbol."). Therefore, it is my opinion that LB-031 discloses this limitation.

c. <u>19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"</u>

237. In my opinion, LB-031 discloses limitation 19[c]. *See, e.g.*, LB-031, pp. 2-3.

238. LB-031 describes the use of VDSL2 transceivers, a VTU-O and a VTU-R. *Id.* at p. 3. LB-031 also discloses the use of an interleaver in a transmitter and a deinterleaver in a receiver. *Id.* at p. 2. One of ordinary skill in the art would have understood, therefore, that LB-031 discloses multiple latency paths within a VTU-O or VTU-R, namely, a downstream path and an upstream path in each. I understand that the Court has construed the term "latency path" to mean "transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay." LB-031 further discloses that an interleaving function is associated with a first latency path, and a deinterleaving function is associated with a second latency path because

the VTU-O has an interleaver in the downstream latency path and a deinterleaver in the upstream latency path, and the VTU-R has an interleaver in the upstream latency path and a deinterleaver in the downstream latency path. LB-031 also describes that the operation of convolutional interleaver/deinterleaver pairs imposes a delay (or latency) on their respective latency paths, which may be different for the different latency paths. *Id.* at 2. Thus, LB-031 discloses that the VTU-O and VTU-R are both multicarrier communications transceivers that are configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path.

d. **19[d]. "the multicarrier communications transceiver being associated with a memory"**

239. In my opinion, LB-031 discloses limitation 19[d]. *See, e.g.*, LB-031, p. 3.

240. LB-031 describes an interleaver memory associated with a VDSL2 transceiver. *Id.* at p. 3 ("The size of the interleaver memory will be a major source of complexity in VDSL2."). LB-031 further explains that the amount of memory required is "implementation specific," and provides examples of the amounts of delay and the amounts of memory required to support them. *Id.* at 3, 4. Therefore, LB-031 discloses that the multicarrier communications transceiver is associated with a memory.

e. **19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"**

241. LB-031 discloses limitation 19[e], in my opinion. *See, e.g.*, LB-031, pp. 3, 6.

242. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this

limitation, however, then LB-031 discloses this limitation under such an interpretation of the claims.

243. LB-031 states that "[d]uring initialization, the VDSL2 transceiver would indicate" its capabilities, and that these capabilities include the maximum bit rate it can support, the maximum supported end-to-end delay in octets, and the maximum delay in ms. LB-031 at pp. 4, 6. LB-031 states that "[t]he requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate," but that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," in which case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities." *Id.* at 3. LB-031 discloses that "[f]or interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets." *Id.* at 3; *see also* 6 ("interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R; the delay in octets should meet the minimum requirements in terms of delay in time."). One of ordinary skill in the art would have understood that this information would be exchanged as part of a message received during initialization, because the "interleaver delay" would be exchanged prior to the receivers entering Showtime and exchanging user data. *See also id.* at 4 ("During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.").

244. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function." LB-031 also discloses how "the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the

interleaver/deinterleaver," and that "for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at LB-031 at p. 2. LB-031 explains that the end-to-end delay of the interleaver/deinterleaver depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* Given that the VTU-O and VTU-R in LB-031 receive a message containing the total delay of the interleaver/deinterleaver, one of ordinary skill in the art would have understood that LB-031 discloses allocating the memory between an interleaving function and a deinterleaving function, within TQ Delta's interpretation of the claims.

f. <u>19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"</u>

245. LB-031 discloses limitation 19[f] in my opinion. *See, e.g.*, LB-031, p. 3,

246. LB-031 discloses interleaving and deinterleaving for VDSL transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits downstream and receives upstream at the same time, and the VTU-R transmits upstream and receives downstream at the same time). Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

B. <u>The Asserted Claims Are Obvious Over the Combination of LB-031 and Mazzoni</u>

247. To the extent it is determined that LB-031 does not render obvious claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, or claim 19 of the '473 patent, it is my opinion that these claims are obvious over LB-031 in combination with U.S. Patent No. 7,269,208 ("Mazzoni"). I have reviewed TQ Delta's infringement contentions for

Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then LB-031 in combination with Mazzoni renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of LB-031

248. I provided a brief description of LB-031 above in Section IX.A.2, which I incorporate by reference.

2. Brief Description of Mazzoni

249. Mazzoni describes a multicarrier transceiver with a shared memory that performs interleaving and deinterleaving and can be used in VDSL communication systems. *See*, *e.g.*, Mazzoni, at col. 1:8-15 ("the invention relates to sending and receiving digital data that can have different bit rates, and to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates"); *id.* at col. 1:19-22 ("The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications"); *id.* at col. 1:54-58 ("Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates."); *id.* at col. 1:59-65 ("These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).").

250. Mazzoni's multicarrier transceiver includes a channel coding/decoding stage that incorporates interleaving and deinterleaving functionality. *See, e.g.*, Mazzoni, col. 2:3-6. The interleaving and deinterleaving elements of the transceiver include a memory whose minimum size "is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system)." *Id.* at col. 2:6-10. The memory assigns spaces to each of the interleaving and deinterleaving means, the sizes of which are set as functions of the bit rates that are processed. *Id.* at col. 2:6-15. Mazzoni recognizes that as a result of this configuration, it is "possible to considerably reduce the size of the memory means required for the interleaving and deinterleaving means implemented within a modem. . . ." *Id.* at col. 2:15-22; *see also id.* at col. 1:65-2:2 ("advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)," such that Mazzoni's invention "is capable of processing different bit rates from a group of predetermined bit rates").

251. Mazzoni notes that "the channel coding/decoding stage may include Reed-Solomon coding/decoding means of length N (where N=240 bytes, for example)." *Id.* at col. 2:37-39; *see also id.* at 2:25-27 ("The transmitted data stream may be protected from transmission channel noise by a Reed-Solomon coding algorithm, which is well known in the art"); *id*. at col. 2:27-37 (noting that the interleaving means may interleave the bytes temporally by modifying the order in which they are transmitted).

252. Mazzoni further describes how the capacity of the memory assigned to the interleaving/deinterleaving means "may need to be chosen in accordance with the maximum bit

rate of the services offered, here the bit rate of the highest asymmetrical service (service A6)." *Id.* at col. 4:18-22. Mazzoni's transceiver thus includes a channel coding unit "CC," which includes Reed-Solomon (RS) coding means associated with the interleaving means. *Id.* at col. 4:36-41. The RS coding is applied individually to each of the data packets delivered to the input of the coding unit CC. *Id.* at col. 4:42-44.

253. Mazzoni's interleaving and deinterleaving functionality includes "I branches of i-1 blocks of M bytes for interleaving and I' branches of I'-1 blocks of M' bytes for deinterleaving," and thus is capable of allocating the shared memory to the interleaver for use at the same time as the shared memory is allocated to the deinterleaver. *Id.* at col. 5:15-20; FIGS. 4-5. The parameters I, M, I' and M' define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. *Id.* at col. 5:24-27. The allocation is accomplished "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M')." *Id.* at col. 5:27-30.

254. FIGS. 4 and 5 of Mazzoni, copied below, illustrate, respectively, the interleaving means and the deinterleaving means. *Id.* at col. 6:15-17.

FIG.4

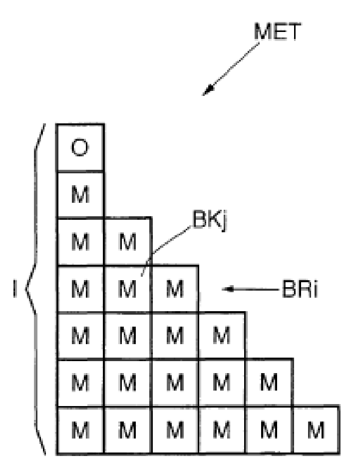
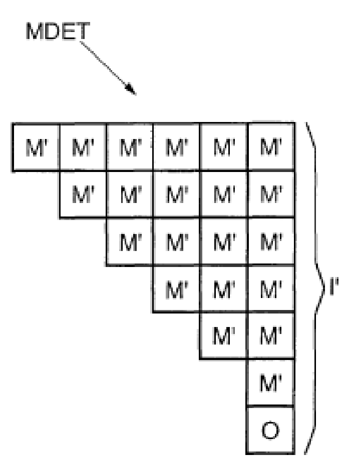
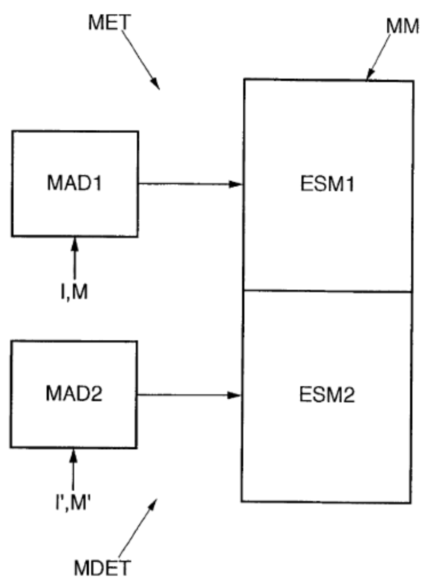


FIG.5



255. FIG. 6 of Mazzoni, copied below, reflects the asymmetrical service, which produces an allocation of shared memory to the interleaver and deinterleaver in which I and I' and M and M' are generally different (*see id.* at col. 5:58-60).

FIG.6



The interleaving means and the deinterleaving means shown in FIG. 6 include common memory means MM, e.g., a dual-port random access memory, and the "memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET." *Id.* at col. 5:61-67

256. Mazzoni's parameters I, I', M and M' used for allocation of the shared memory can be determined from maximum and minimum memory size capacities that are easily calculable using downlink and uplink bit rates, the number of bits affected by noise, and RS error correction. *Id.* at col. 6:19-50. The size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to Ix(I-l)xM/2. *Id.* at col. 6:38-41. Similarly, the size of the second memory space ESM2 required to

support the uplink bit rate is equal to I'x(I'-l)xM'/2, where I and I' are submultiples of the size N of the RS code. *Id.* at col. 6:41-44.

3. Claim 1 of the '048 Patent

257. It is my opinion that LB-031 in combination with Mazzoni discloses each limitation of claim 1 of the '048 Patent.

a. 1[a]. "A system that allocates shared memory"

258. It is my opinion that LB-031 in combination with Mazzoni discloses the preamble, limitation 1[a] of claim 1 of the '048 patent, to the extent that it is limiting. *See, e.g.*, LB-031 at p. 3; Mazzoni, col. 1:54-65; col. 2:3-21; col. 5:58-67.

259. LB-031 discloses allocating shared memory between an interleaver and a deinterleaver in a VDSL system, as I describe above in Section IX.A.3.a, which I incorporate by reference.

260. Mazzoni also discloses a system that allocates shared memory. I note that the Court construed "shared memory" as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Mazzoni explains that its disclosures can be applied to a VDSL environment or system. Mazzoni, col. 1:19-22 ("The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications."). In a VDSL environment, Mazzoni describes "an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates." *Id.* at col. 1:54-59. Mazzoni further discloses that it provides a memory that "can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive

device (modem)." *Id*. at col. 1:61-65. As Mazzoni further describes, "[t]he memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means." *Id.* at col. 2:3-21; *see also id.* at col. 5:58-67 (describing "common memory means MM, e.g., a dual-port random access memory."). Claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: interleaving and deinterleaving the digital data; setting a minimum size of a shared memory based upon a maximum bit rate of the group of predetermined bit rates; assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data; and the interleaving providing convolutional interleaving of I branches with i−1 blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I′ branches of i′−1 blocks of M′ bytes, with I and I′ being sub-multiples of N and i and i′ being current relative indexes of the branches."

261. Thus, Mazzoni in combination with LB-031 discloses common memory used by an interleaver and a deinterleaver, where a portion of the memory can be used by either one of the two functions.

b. 1[b]. "a transceiver that is capable of"

262. It is my opinion that LB-031 in combination with Mazzoni discloses limitation 1[b]. *See, e.g.*, LB-031, at pp. 3-4; Mazzoni, col. 1:8-27.

263. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have

understood to be VDSL2 transceivers, as described above at Section IX.A.3.b, which I incorporate by reference. *Id.* at 3.

264. Mazzoni similarly discloses its invention "may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system," which a person having ordinary skill in the art would have understood to include VDSL transceivers. Mazzoni, col. 1:19-21. Mazzoni further discloses that its invention can transmit and receive data, as it "provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication systems)." *Id.* at col. 1:65-2:2. Mazzoni provides a depiction of two "send/receive devices TO and TU according to the invention." *Id.* at col. 3:53-61, FIG. 1. One of ordinary skill in the art would have understood these devices to be transceivers.

265. Mazzoni also discloses that in its invention, at least some circuitry is shared between the transmit and receive portions, specifically, a common memory for interleaving and deinterleaving. *Id.* at col. 2:2-13 ("The device according to the invention may include a coding/decoding stage (generally referred to by those skilled in the art as a 'channel coding/decoding stage including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means."). The "memory" associated with the interleaving and deinterleaving means is common circuitry shared by the transmitter and receiver portions.

c. <u>1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver"</u>

266. In my opinion, LB-031 in combination with Mazzoni discloses limitation 1[c]. *See, e.g.*, LB-031, pp. 3, 6; Mazzoni, col. 1:19-27.

267. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, or with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then LB-031 in combination with Mazzoni discloses this limitation under such an interpretation of the claims.

268. LB-031 discloses that "the VTU-O and VTU-R must exchange the interleaver delay in terms of octets," and the relationship between the interleaver delay in octets and the amount of interleaver memory needed. *Id.* at 3; *see also* 6 ("interleaver delay in terms of octets should be exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time."). I discuss how LB-031's message meets this limitation above at Section IX.A.3.c, which I incorporate by reference.

269. In addition, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. The system according to Mazzoni then divides the memory between the interleaving and deinterleaving means. *Id.* at col. 5:64-67 ("The

memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 in assigned to the deinterleaving means MDET."). The size of the memory space is selected based on the bit rate. *Id.* at col. 6:26-30 ("The size of the memory space needed to store this maximum bit rate is then equal to Nxnrs/2, where N is the size of the Reed-Solomon code (here 240). The resulting memory space size is therefore equal to 24,960 bytes."). One of ordinary skill in the art would have understood that the bit rate information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, as is described in LB-031. Thus, LB-031 in combination with Mazzoni discloses limitation 1[c] under TQ Delta's interpretation of the claims.

d. <u>1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory"</u>

270. LB-031 in combination with Mazzoni discloses limitation 1[d], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4; Mazzoni, col. 1:46-2:2; col. 2:6-17; col. 2:25-36; col. 4:18-22; col. 5:21-30; col. 5:58-67; col. 6:19-50.

271. LB-031 describes how a transceiver can determine an amount of memory required by an interleaver to interleave Reed Solomon coded data bytes within the shared memory. I explain this in Section IX.A.3.d above, which I incorporate by reference.

272. Mazzoni also discloses this limitation. For example, Mazzoni explains that "the parameters I, M, I′ and M′ can be modified, e.g., by software, and are delivered by control means MCD," and that "[t]hese parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means." Mazzoni at col. 5:21-27. Claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . setting a

minimum size of a shared memory based upon a maximum bit rate of the group of predetermined bit rates. . . .”

273. Thus, LB-031 in combination with Mazzoni discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

e. **<u>1[e]. “allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate”</u>**

274. It is my opinion that LB-031 and Mazzoni disclose limitation 1[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50; col. 10:22-42.

275. LB-031 describes allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. I explain this in Section IX.A.3.e above, which I incorporate by reference.

276. Mazzoni also discloses this limitation. For example, Mazzoni explains that “the parameters I, M, I′ and M′ can be modified, e.g., by software, and are delivered by control means MCD,” and that “[t]hese parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means.” Mazzoni at col. 5:21-27. The bytes to be interleaved are bytes of a Reed-Solomon codeword. *Id.* at col. 4:36-41 (“The channel coding unit CC includes Reed-Solomon coding means whose structure and function are known to those of skill in the art. The Reed-Solomon coding means are associated with the interleaving means. In conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel. Reed-Solomon coding is applied

individually to each of the data packets delivered to the input of the coding unit CC."); *id.* at col. 6:11-18 ("An example of the capacity of the memory MM and of the values chosen for the parameters I, M, I′ and M′ for an asymmetrical service A6 and an RS (240, 224) Reed-Solomon code with a correction power of 8 bytes/word may be as follows when the transmission lines are disturbed by an impulsive noise with a duration of 0.25 ms.").

277. Mazzoni discloses implementing the interleaver using "I parallel branches BRi (numbered from 0 to I−1, for example) which are implemented with a delay increment of M per branch (M represents the maximum number of bytes of a block BKj with index j)." *Id.* at col. 5:31-35; *see also id.* at col. 6:19-30. The bytes are then interleaved, which means a first number of bytes of the shared memory to the interleaver were allocated to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. *See, e.g. id.* at col. 5:39-48.

278. Furthermore, claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data. . . ."

279. Therefore, LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

f. 1[f]. "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message"

280. LB-031 in combination with Mazzoni discloses limitation 1[f], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:19-27.

281. I have reviewed TQ Delta's infringement contentions, and I understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, LB-031 in combination with Mazzoni discloses this limitation in my opinion.

282. LB-031 discloses that the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. I explain this in Section IX.A.3.f above, which I incorporate by reference.

g. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

283. In my opinion, LB-031 and Mazzoni disclose limitation 1[g]. *See, e.g.*, LB-031, pp. 2-3, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50; col. 10:22-42; Fig. 3.

284. LB-031 discloses allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate. I explain this in Section IX.A.3.g above, which I incorporate by reference.

285. Mazzoni also discloses allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at

a second data rate. Specifically, Mazzoni discloses that "[t]he deinterleaving means . . . have a structure analogous to that which has just been described for the interleaving means," but "the indices of the branches are reversed so that the longest interleaving time-delay corresponds to the shortest deinterleaving time-delay." Mazzoni at col. 5:49-55. Mazzoni explains that "[t]he deinterleaving means MDET incorporated in the operator terminal TO have I′ branches, the branch with index i′ having a length equal to i′×M′ bytes." *Id.* at col. 5:55-57. Claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: . . . assigning a first memory space of the shared memory for interleaving and a second memory space of the shared memory for deinterleaving, a size of each of the first and second memory spaces being set as a function of the bit rate actually processed by the device; performing Reed-Solomon coding and decoding for a length N of the digital data; . . . ."

286. Therefore, it is my opinion that LB-031 and Mazzoni both disclose allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate.

h. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

287. In my opinion, LB-031 and Mazzoni disclose limitation 1[h]. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 4:36-44; col. 6:51-8:10.

288. LB-031 discloses interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. I explain this in Section IX.A.3.h above, which I incorporate by reference.

289. Mazzoni also discloses interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. For example, Mazzoni discloses that the interleaver operates as follows: "The first block of M bytes (having the index 0, for example) is not interleaved and is delivered unmodified to the output of the interleaving means. The next block of M bytes (index 1) is delivered to the input of the branch BR1, and so on up to the seventh block of M bytes (index 6), which is delivered to the branch BR6. The cycle then begins again with the blocks of bytes with indices from 7 to 13. The preceding blocks of bytes are either delivered to the output of the interleaving means or moved forward by one block BKj in the branch concerned." Mazzoni at col. 5:39-48; *see also id.* at FIG. 4. Mazzoni explains that the deinterleaver operates similarly. *Id.* at col. 5:49-57.

290. FIGS. 4 and 5 of Mazzoni, copied below, and the associated text illustrate the process of interleaving and deinterleaving.

FIG.4

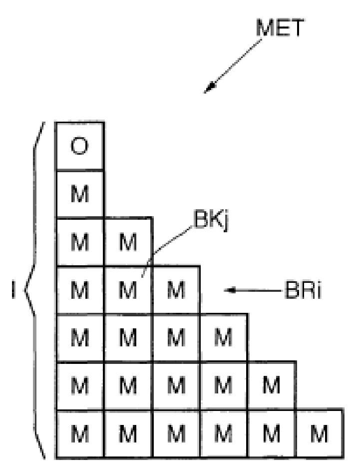
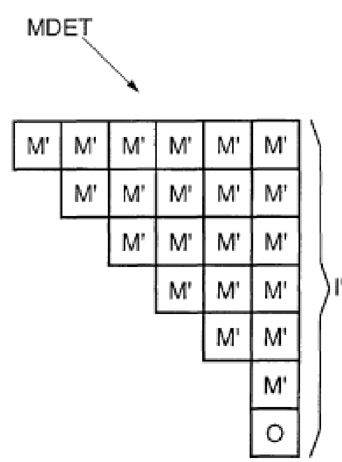


FIG.5



291. In addition, claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the

method comprising: interleaving and deinterleaving the digital data; . . . performing Reed-Solomon coding and decoding for a length N of the digital data; and the interleaving providing convolutional interleaving of I branches with i−1 blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I′ branches of i′−1 blocks of M′ bytes, with I and I′ being sub-multiples of N and i and i′ being current relative indexes of the branches."

292. Therefore, in my opinion, LB-031 and Mazzoni disclose interleaving the first plurality of RS coded data bytes within the shared interleaver memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

i. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

293. It is my opinion that LB-031 and Mazzoni disclose limitation 1[i]. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-65; col. 6:21-30; col. 5:61-67; col. 10:22-42; col. 3:43-48; col. 6:51-8:10; Fig. 7, 8.

294. LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I explain this in Section IX.A.3.i above, which I incorporate by reference.

295. Mazzoni also discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I understand that the Court has construed the term "the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]" as "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." Mazzoni

discloses that the shared memory is a dual-port memory. *See, e.g.*, Mazzoni at col. 2:57-58 ("The memory may be a random access memory, such as a dual-port memory, for example."); *id.* at col. 5:58-67 ("the interleaving means and the deinterleaving means include common memory means MM, e.g., a dual-port random access memory. The memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET, and a second memory space ESM2 is assigned to the deinterleaving means MDET."); claim 7 ("The device according to claim 1 wherein said memory comprises a dual-port memory."); claim 12 ("The device according to claim 8 wherein said random access memory comprises a dual-port memory."). As would have been appreciated by a person having ordinary skill in the art as of the Family 3 patents' priority date, a dual-port memory is a memory that can be read from and written to at the same time. Through this disclosure, a skilled artisan would have understood Mazzoni to disclose that the shared memory allocated to the interleaver is read to, written from, or holds data at the same time as the shared memory allocated to the deinterleaver is read to, written from, or holds data.

296. In addition, claim 13 of Mazzoni recites "[a] method for sending and receiving digital data and processing different bit rates from a group of predetermined bit rates, the method comprising: interleaving and deinterleaving the digital data; . . . and the interleaving providing convolutional interleaving of I branches with i−1 blocks of M bytes, and the deinterleaving providing convolutional deinterleaving with I′ branches of i′−1 blocks of M′ bytes, with I and I′ being sub-multiples of N and i and i′ being current relative indexes of the branches."

297. Thus, LB-031 and Mazzoni both disclose that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

Consequently, the combination of LB-031 and Mazzoni discloses every limitation of claim 1 of the ’048 patent.

4. <u>Claim 5 of the ’381 Patent</u>

298. It is my opinion that claim 5 of the ’381 patent is rendered obvious by LB-031 in combination with Mazzoni.

a. <u>5[a]. “A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver”</u>

299. To the extent that it is limiting, it is my opinion that LB-031 discloses the preamble. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:8-27; col. 1:54-65; col. 1:59-65; col. 2:3-21; col. 5:58-67.

300. LB-031 discloses the use of an interleaver pair in a VDSL2 VTU-O and VTU-R. *See id.* at p. 3. Similarly, Mazzoni discloses a VDSL transceiver that includes a channel coder/decoder. *See* Mazzoni, col. 1:8-27; col. 2:3-19. One of ordinary skill in the art would have understood that source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code. I discuss how LB-031 in combination with Mazzoni discloses allocating shared memory in a transceiver above with respect to claim 1 of the ’048 patent, which I incorporate here by reference. *See* Section IX.B.3.a. I describe how LB-031 in combination with Mazzoni discloses a transceiver above at Section IX.B.3.b, which I also incorporate by reference. Thus, LB-031 and Mazzoni disclose the preamble of claim 5.

b. <u>5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"</u>

301. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[b]. *See, e.g.*, LB-031, pp. 3, 4, 6; Mazzoni, col. 1:19-27.

302. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation. If the Court or other trier of fact interprets the claim such that sending or receiving the O-PMS message meets this limitation, however, then the combination of LB-031 and Mazzoni discloses this limitation under such an interpretation of the claims.

303. Above at Section IX.B.3.c, I describe how LB-031 in combination with Mazzoni discloses this limitation, and I incorporate this discussion by reference. Further, LB-031 discloses that "[t]ypically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at 2. One of ordinary skill in the art would have understood that the relationships described in LB-031 between delay, interleaver memory size, data rate and other transmission parameters are for an interleaver or a deinterleaver. In addition, Mazzoni notes that "everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I' branches." Mazzoni, col. 8:3-5. Thus its discussion of the process for allocating memory to an interleaver would be equally applicable to a deinterleaver. Thus is it my opinion that LB-031 in combination with Mazzoni discloses this limitation.

c. <u>5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"</u>

304. LB-031 in combination with Mazzoni discloses limitation 5[c], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 4; Mazzoni, col. 1:46-2:2; col. 2:6-17; col. 2:25-36; col. 4:18-22; col. 5:21-30; col. 5:58-67; col. 6:19-50.

305. Above at Section 269, I describe how LB-031 in combination with Mazzoni discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my discussion and opinions by reference. LB-031 discloses the relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. *See id.* at p. 3. Mazzoni discloses determining an amount of memory based on a data rate. Mazzoni, col. 4:18-22; col. 5:21-30. Accordingly, LB-031 in combination with Mazzoni discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. <u>5[d]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"</u>

306. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[d]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 5:21-30; col. 5:61-67; col. 6:19-50, col. 10:22-42.

307. Above at Section IX.B.3.e, I explain how LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In

addition, at Section 282 above, I explain how LB-031 in combination with Mazzoni discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of these discussions by reference, and on that basis, it is my opinion that LB-031 in combination with Mazzoni discloses this limitation.

e. **5[e]. "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"**

308. In my opinion, LB-031 in combination with Mazzoni discloses limitation 5[e]. *See, e.g.*, LB-031, pp. 2-3, 4, 5, 6; Mazzoni, col. 1:19-27.

309. I have reviewed TQ Delta's infringement contentions, and understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's infringement position. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, LB-031 in combination with Mazzoni discloses this limitation in my opinion.

310. Above at Section IX.B.3.f, I explain how LB-031 discloses wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message, and I incorporate that discussion by reference. In the same way that the VTU-O or VTU-R of LB-031 and Mazzoni would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than in specified in the messages that it exchanges during initialization, in my opinion.

f. 5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"

311. LB-031 in combination with Mazzoni discloses limitation 5[f], in my opinion. *See, e.g.*, LB-031, pp. 2-3, 5, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 6:19-50; col. 5:61-67; col. 10:22-42; Fig. 6.

312. Above at Section 282, I explain how LB-031 with Mazzoni allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.B.3.e above, I explain how LB-031 and Mazzoni disclose allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and, on that basis, it is my opinion that the combination of LB-031 and Mazzoni discloses limitation 5[f].

g. 5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"

313. LB-031 in combination with Mazzoni, in my opinion, discloses limitation 5[g]. *See, e.g.*, LB-031, p. 3, 6; Mazzoni, col. 1:59-65; col. 2:6-17; col. 2:25-36; col. 4:36-44; col. 6:51-8:10.

314. Above at Section IX.B.3.h, I explain how LB-031 in combination with Mazzoni discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a

transceiver would implement this limitation. It is my opinion that LB-031 in combination with Mazzoni discloses this limitation.

h. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

315. LB-031 in combination with Mazzoni discloses limitation 5[h], in my opinion. *See, e.g.*, LB-031, pp. 3, 6; Mazzoni, col. 1:59-65; col. 6:21-30; col. 5:61-67; col. 10:22-42; col. 3:43-48; col. 6:51-8:10.

316. I explain above at Section IX.B.3.i how it is my opinion that LB-031 and Mazzoni disclose wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference in these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by LB-031 and Mazzoni.

5. Claim 13 of the '882 patent

317. In my opinion, LB-031 in combination with Mazzoni discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. "A system that allocates shared memory"

318. To the extent that this preamble is limiting, LB-031 in combination with Mazzoni discloses a system that allocates shared memory. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:54-65; col. 2:3-21; col. 5:58-67. This limitation is identical to the preamble of Claim 1 of the '048 patent, and, for the same reasons, it is my opinion that this limitation is disclosed by LB-031 and Mazzoni. *See* Section IX.B.3.a.

b. <u>13[b]. "a transceiver that performs"</u>

319. In my opinion, LB-031 in combination with Mazzoni discloses limitation 13[b]. *See, e.g.*, p. 3, 4; Mazzoni, col. 1:8-27. This limitation is identical to the second limitation of Claim 1 of the '048 patent, except that it recites "a transceiver capable of" additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.B.3.b, and I incorporate my discussion and opinions herein by reference.

c. <u>13[c] through 13[i]</u>

320. Limitations 13[c] through 13[i] of claim 13 of the '882 patent are substantially identical to limitations 5[b] through 5[h] of claim 5 of the '381 patent. *See* Appx. 3 (comparing claim limitations of claim 13 of the '882 patent with claim limitations of claim 5 of the '381 patent). I incorporate by reference my opinions with respect to those limitations set forth in Sections IX.B.3.c through IX.B.3.i (claim 1) and Sections IX.B.4.b through IX.B.4.h (claim 5). For the same reasons, it is my opinion that limitations 13[c] through 13[i] are met by LB-031 and Mazzoni.

6. <u>Claim 19 of the '473 Patent</u>

321. In my opinion, claim 19 of the '473 patent is obvious over LB-031 in combination with Mazzoni.

a. <u>19[a]. "An apparatus comprising"</u>

322. To the extent that the preamble is limiting, LB-031 and Mazzoni discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, LB-031, pp. 3, 4.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

323. It is my opinion that LB-031 in combination with Mazzoni discloses limitation 19[b]. *See, e.g.*, LB-031, pp. 3, 4; Mazzoni, col. 1:8-27.

324. LB-031 describes the use of a VDSL2 VTU-O and VTU-R to implement its equations and systems for allocating memory, which one of ordinary skill in the art would have understood to be VDSL2 transceivers. *Id.* at 3. LB-031 further provides an example of calculating and allocating interleaver memory in a VDSL2 transceiver. *Id.* at 4. I understand that the Court construed the term "transceiver" to mean "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry." One of ordinary skill in the art would have understood that VDSL2 transceivers described in LB-031 both transmit and receive data (i.e., to be interleaved and deinterleaved), and share common circuitry such as a memory.

325. LB-031 generally deals with VDSL2, which one of ordinary skill in the art would have understood to be a multicarrier communications system. Moreover, LB-031 describes the use of DMT symbols, and one of ordinary skill in the art would have understood DMT to be a type of multicarrier communications system. LB-031 at p. 4 ("Similar to the interleaver delay, we propose that the maxiumum number of codewords in a DMT symbol (or per unit time) also scale with the data rate).

326. Mazzoni similarly discloses its invention "may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system," which a person having ordinary skill in the art would have understood to include VDSL2 transceivers. Mazzoni, col. 1:19-21. Mazzoni further discloses that its invention can transmit and receive data, as it "provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication systems)." *Id.* at col. 1:65-2:2. Mazzoni provides a depiction of two "send/receive devices TO and TU according to the invention." *Id.* at col. 3:53-

61, Fig. 1. One of ordinary skill in the art would have understood these devices to be transceivers.

327. Mazzoni also discloses that in its invention, at least some circuitry is shared between the transmit and receive portions, specifically, a common memory for interleaving and deinterleaving. *Id.* at col. 2:2-13 ("The device according to the invention may include a coding/decoding stage (generally referred to by those skilled in the art as a 'channel coding/decoding stage') including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means."). The "memory" associated with the interleaving and deinterleaving means is common circuitry shared by the transmitter and receiver portions.

328. Mazzoni further discloses a VDSL system, which one of ordinary skill in the art would have understood to include a multicarrier communications transceiver.

c. **19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"**

329. In my opinion, LB-031 in combination with Mazzoni discloses limitation 19[c]. *See, e.g.*, LB-031, pp. 2-3; Mazzoni, col. 3:62-4:25.

330. LB-031 describes the use of VDSL2 transceivers, a VTU-O and a VTU-R. *Id.* at p. 3. I understand that the Court has construed the term "latency path" to mean "transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay." One of ordinary skill in the art would have understood that LB-031 discloses a multiple latency paths within a VTU-O or VTU-R, because a VTU-O transmits data downstream and receives

data upstream, and, similarly, a VTU-R transmits data upstream and receives data downstream. LB-031 describes that the operation of convolutional interleaver/deinterleaver pairs imposes an end-to-end interleaver delay (or latency) on their respective latency paths. *Id.* at 2. Thus, one of ordinary skill in the art would have understood LB-031 to disclose at least two latency paths, one downstream and one upstream.

331. Mazzoni discloses that "the VDSL communication system enables the operator to provide symmentrical services, typically six symmetrical services S1-S6." Mazzoni, col. 3:62-64. Mazzoni also discloses that "the operator can also provide asymmetrical services A1-A6. These are services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction)." *Id.* at col. 4:3-7. One or ordinary skill in the art would have understood the disclosure of asymmetrical and symmetrical services to require multiple latency paths (i.e., at least one latency path in the downstream direction and at least one latency path in the upstream direction), and, in turn, interleaving and deinterleaving functions for the respective latency paths.

d. 19[d]. "the multicarrier communications transceiver being associated with a memory"

332. In my opinion, LB-031 in combination with Mazzoni discloses limitation 19[c]. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-2:24; col. 2:37-48; col. 2:57-3:4; col. 5:9-20; Fig. 3, 4, 5.

333. LB-031 describes an interleaver memory associated with a VDSL2 transceiver. LB-031 at p. 3 ("The size of the interleaver memory will be a major source of complexity in VDSL2."); *see also id.* at p 2 ("the smallest possible memory for either the interleaver or deinterleaver is [half of the overall delay of the interleaver/deinterleaver pair]"). LB-031 further explains that the amount of memory required is "implementation specific," and provides

examples of delay constraints/requirements and the amounts of memory required to support them. *Id.* at 3, 4.

334. Mazzoni similarly discloses a memory associated with the multicarrier communications transceiver. Mazzoni, col. 2:6-10 ("The interleaving and deinterleaving means include a memory whose minimum size is a function of the maximum bit rate of the group of predetermined bit rates (e.g., the highest asymmetrical bit rate in the case of a VDSL system)."); col. 2:57-60 ("The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means."); *see also id.* at Fig. 4, 5. Thus, Mazzoni in combination with LB-031 discloses this limitation.

e. 19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

335. LB-031 in combination with Mazzoni discloses limitation 19[e], in my opinion. *See, e.g.*, LB-031, pp. 3, 6; Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30.

336. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then LB-031 in combination with Mazzoni discloses this limitation under TQ Delta's interpretation of the claims.

337. LB-031 discloses that "the VTU-O and VTU-R must exchange the interleaver delay in terms of octets." *Id.* at 3; *see also* 6 ("interleaver delay in terms of octets should be

exchanged between the VTU-O and VTU-R, the delay in octets should meet the minimum requirements in terms of delay in time."). One of ordinary skill in the art would have understood that this information would be exchanged as part of a message received during initialization, because the "interleaver delay" would be exchanged prior to the receivers entering Showtime and exchanging user data. Furthermore, LB-031 discloses the VDSL2 transceivers indicating their capabilities during initialization. *See id.* at 4 ("During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay.").

338. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function." LB-031 discloses that "the smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver, and that "for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same." *Id.* at LB-031 at p. 2. LB-031 also explains the dependence of end-to-end delay of the interleaver/deinterleaver pair depends on line rate, Reed Solomon codeword size, and other parameters. *Id.* One of ordinary skill in the art would have understood that LB-031 discloses allocating the memory between an interleaving function and a deinterleaving function using the total delay of the interleaver/deinterleaver pair in the downstream direction and using the total delay of the interleaver/deinterleaver pair in the upstream direction.

339. In addition, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses

that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. One of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message.

f. **<u>19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"</u>**

340. LB-031 in combination with Mazzoni discloses limitation 19[f] in my opinion. *See, e.g.*, LB-031, p. 3; Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30.

341. LB-031 discloses interleaving and deinterleaving for VDSL2 transceivers. *See, e.g.*, LB-031 at pp. 1-3. As a person having ordinary skill in the art as of the priority date of the Family 3 patents would have understood, VDSL transceivers transmit and receive data at the same time (i.e., the VTU-O transmits downstream and receives upstream at the same time, and the VTU-R transmits upstream and receives downstream at the same time). Thus, LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

342. In addition, LB-031 discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message. *See, e.g.*, LB-031 at p. 3 ("the VTU-O and VTU-R must exchange the interleaver delay in terms of octets."); *id.* at p. 4 ("During initialization, the VDSL2 transceiver would

indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay."); *id.* at p. 2 ("the smallest possible memory for either the interleaver or deinterleaver is [half of the overall delay of the interleaver/deinterleaver pair]").

343. Mazzoni also discloses a memory that can be shared between the interleaving and deinterleaving means. Mazzoni, col. 1:59-65 ("These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)."); col. 2:57-50 ("The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respectively include first addressing means and second addressing means."). One of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time.

344. Mazzoni also discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message. For example, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31.

7. Motivation to Combine LB-031 and Mazzoni

345. As of the priority date of the Family 3 patents, a person having ordinary skill in the art would have been motivated to combine the teachings of Mazzoni with the teachings of LB-031 in the manner recited in the asserted claims.

346. First, both Mazzoni and LB-031 disclose VDSL transceivers. *See, e.g.*, LB-031 at p. 1 (Title) ("VDSL2 – Constraining the Interleaver Complexity"); *id.* at p. 4 ("During initialization, the VDSL2 transceiver would indicate that it could support up to 44.5 Mbit/s and 29092 or more octets of interleaver delay."); Mazzoni at col. 1:19-22 ("The present invention may advantageously be applied to a very high rate digital subscriber line (VDSL) environment or system, for example, though the invention may also be used in other applications.").

347. Second, both Mazzoni and LB-031 are concerned with limiting the size of memory used for interleaving and deinterleaving. *See, e.g.*, LB-031 at p. 1 ("The interleaver is a major source of complexity in VDSL2. We propose that the interleaver delay in time be restricted rather than restricting the depth as in ADSL2. This allows . . . lower complexity implementations for profiles that do not require the full VDSL2 data rate."); Mazzoni at col. 1:39-43 ("The processes of interleaving and deinterleaving data sent and received by a modem necessitates the use of memories. For a modem intended to operate at a predetermined bit rate, the memories must have a capacity that depends on that bit rate."); *id.* at col. 1:47-49 ("An object of the invention is to provide a send/receive device (i.e., modem) architecture which requires a reduced quantity of memory.").

348. To the extent that LB-031 does not explicitly disclose the use of shared memory to reduce interleaver complexity and cost, Mazzoni describes a method of implementing shared memory to reduce the amount of memory required. As of the priority date of the Family 3

patents, one of ordinary skill in the art would have been motivated to look to Mazzoni, in view of the teachings of LB-031, to reduce the complexity of an interleaver.

349. Mazzoni discloses that the amount of memory required for interleaving and deinterleaving, and therefore the "sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means," depends on the downstream and upstream interleave depth (denoted in Mazzoni as I for the interleaver and I′ for the deinterleaver), block length (denoted in Mazzoni as M for the interleaver and M′ for the deinterleaver), and bit rates, which can be symmetric or asymmetric. Mazzoni at col. 5:21-30; *id.* at col. 2:19-24. *See also id.* at col. 2:13-15 ("The size of each of the two memory spaces is set as a function of the bit rate actually processed by the device."). As a person having ordinary skill in the art would have understood, the parameters I, M, I′ and M′ would need to be chosen so as not to exceed the size of the shared memory given the bit rate processed by the transceiver.

350. LB-031 teaches the VTU-O and VTU-R exchanging the interleaver delay in terms of octets for this exact reason, i.e., so that the VTU-O and VTU-R can then "select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities." LB-031 at p. 3. Like Mazzoni, LB-031 also teaches that the amount of memory required for interleaving and deinterleaving depends on the line data rate. *Id.* at p. 4. Thus, a skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have been motivated to include the initialization message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I, M, I′ and M′ that would not exceed the size of the shared memory at the selected downstream and upstream bit rates.

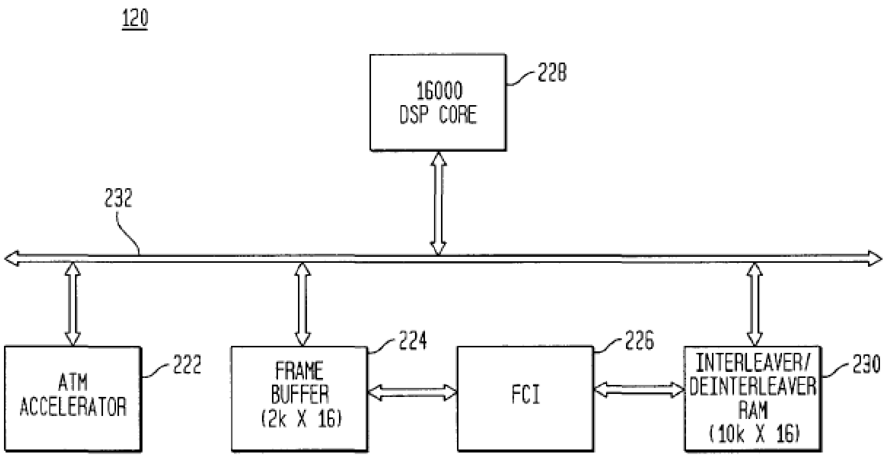
C. The Asserted Claims Are Obvious Over Fadavi-Ardekani in Combination With ITU-T Recommendation G.993.1

351. It is my opinion that U.S. Patent No. 6,707,822 (Fadavi-Ardekani), in combination with either ITU-T Recommendation G.993.1 ("G993.1") renders obvious each of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent. Furthermore, one of ordinary skill in the art would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1, as I describe below in Section IX.C.7. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions, and I do not agree with its infringement read. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Fadavi-Ardekani in combination with G.993.1 renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of Fadavi-Ardekani

352. Fadavi-Ardekani describes a transceiver for asymmetric communication systems, such as ADSL, that implements a buffering and scheduling scheme to allow a single transceiver to synchronize data processing between multiple asynchronous ADSL sessions corresponding to different ADSL lines. Fadavi-Ardekani at Abstract; col. 2:47-67. FIG. 2 of Fadavi-Ardekani, copied below, shows an ADSL transceiver in accordance with Fadavi-Ardekani's invention. *Id.* at col. 3:65-67.

FIG. 2



353. The transceiver includes three functional elements (a DSP core, a framer/coder/interleaver (FCI), and an ATM accelerator) and two memories (a frame buffer (FB) and an interleave/deinterleave memory (IDIM)) coupled together. *Id.* at col. 3:5-7; col. 5:23-28. The DSP core generates a virtual clock signal that is used to synchronize the signal processing tasks of the transceiver, i.e., to control the operation of the ATM accelerator and the FCI. *Id.* at col. 3:7-8; col. 3:20-23; col. 6:27-29. The virtual clock signal has a frequency of approximately 4 kHz, which is the DMT symbol rate in ADSL. *Id.* at col. 3:20-23; col. 6:29-31. The DSP core controls operation of both the ATM accelerator and the FCI, and it manages the transfer of data to and from the FB and IDIM. *Id.* at col. 3:23-25.

354. The ATM accelerator "provides the network interface to multiple ATM channels for multiple asynchronous ADSL sessions." *Id.* at col. 3:8-11. It "provides those functions that are responsible for data transport for a plurality of data streams communicated via twisted pair media." *Id.* at col. 5:41-45. Among other things, the ATM accelerator assigns data to an appropriate bearer channel "as determined by the ADSL standard," "subjects this framed data to various operations that calculate a plurality of complex numbers representing DMT tones," and "subsequently transfers this DMT tone data on the twisted-pair media." *Id.* at col. 5:45-54.

355. The FCI performs various processing tasks on the frame data that are required by the ADSL standards, including "framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/de-scrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving." *Id.* at col. 6:11-16; col. 6:19-20. A preferred embodiment of the FCI is able to support approximately four T1.413 Issue 2 sessions (i.e., lines) or four G.992.2 sessions at one time. *Id.* at col. 6:20-23.

356. The FB provides a dual access memory used by the DSP core to transfer unframed bearer channel data between the ATM accelerator and the FCI. *Id.* at col. 5:57-60.

357. The IDIM provides a memory used by the DSP core to transfer data frames to and from the FCI for interleaving and deinterleaving. *Id.* at col. 6:55-60. In addition to storage for interleaving, the IDIM may include a dedicated area enabling the transfer of fast path data (i.e., non-interleaved data) between the FCI and the DSP core. *Id.* at col. 60-62. Fadavi-Ardekani teaches that "[t]he size of the IDIM and the interleave depth [of the ADSL sessions] may be varied so that a different number of sessions may be supported by the transceiver of the invention." *Id.* at col. 7:3-5. In an "optimal implementation of the interleaver," Fadavi-Ardekani teaches using "the same memory for receive data and transmit data" using a 20-kbyte IDIM, which is sufficient to support "a standard ADSL session at full interleave depth" or more than one session with each using a smaller interleave depth. *Id.* at col. 7:25-32.

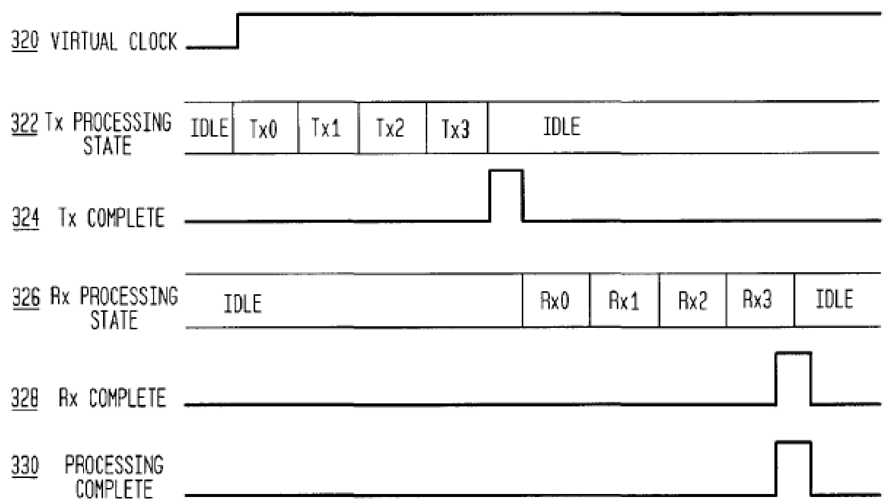
358. Both the FB and IDIM are used in what Fadavi-Ardekani refers to as "a ping-pang fashion, based on the logic level of the virtual clock." *Id.* at col. 3:13-17; col. 6:57-58. "Ping-pang fashion" means that "areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent." *Id.* at col. 5:60-63. Fadavi-Ardekani explains that within a common memory, "[a]s one

area of memory is being used by a first agent, another area of memory can be used by a different agent," and "[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors." *Id.* at col. 5:63-6:1. At any given time, "an agent is allowed to access either a ping area of memory or a pang area of memory based on the logic level of the virtual clock signal." *Id.* at col. 6:1-4.

359. In operation, during each virtual clock cycle, the transceiver completes a sequence that processes the data associated with however many lines are connected to the transceiver, including both the transmit ("TX") data and the receive ("RX") data. *Id.* at col. 7:46-53; col. 7:63-8:4. For interleaving and deinterleaving, "the DSP core needs to load one or more frames of RX [receive] data to the IDIM and read one or more frames of TX [transmit] data from the IDIM." *Id.* at col. 7:46-53. As a person having ordinary skill would have understood on the Family 3 patents' priority date, this disclosure means that during each of the virtual clock cycles (i.e., during each DMT symbol period), one frame of receive data for each connected line is loaded to the IDIM for deinterleaving by the FCI, and one frame of transmit data for each connected line is loaded to the IDIM for interleaving by the FCI.

360. FIG. 3 of Fadavi-Ardekani, copied below, illustrates the processing sequence enabling the transceiver to service four lines. *Id.* at col 4:1-2. As shown in FIG. 3, during each virtual clock cycle, "the transceiver first steps through ADSL lines, performing FCI transmit-processes for each active ADSL line and generating a control signal after completing all transmit-processes," and "[t]he FCI then again steps through ADSL lines, processing receive-processes for all active ADSL lines and generating control signals indicating completion of receive processes and completion of all processing." *Id.* at 26-35.

FIG. 3



361. The FCI processing is initiated by the transition of the virtual clock 320, shown as an upward transition in FIG. 3. The FCI begins each virtual clock cycle by processing the transmit data for each line in sequence (shown in the line of FIG. 3 labeled 322). *Id.* at col. 8:22-26. At the end of the TX processing cycle, one frame of transmit data for each line resides in the IDIM. *Id.* at col. 8:30-33. After completing the TX processing cycle (indicated by the pulse shown in the line of FIG. 3 labeled 324), and still within the same virtual clock cycle, the FCI processes the receive data. *Id.* at col. 8:34-35. The FCI steps through each line in sequence (shown in the line of FIG. 3 labeled 326). *Id.* at col. 8:35-37.

362. While the FCI is performing the TX processing during the first part of the virtual clock cycle, "the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:62-65. Similarly, while the FCI block is performing the RX processing during the second part of the virtual clock cycle, "the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:67-9:3.

363. Fadavi-Ardekani was filed as an application on January 7, 2000, and was published when it issued on March 16, 2004. I understand that it is prior art to the Asserted Family 3 Patents.

2. Brief Description of G.993.1.

364. I provide a description of G.993.1 above at Section VII.F.4, which I incorporate here by reference.

365. I understand that G.993.1 was approved no later than June of 2004, although numerous prior versions of G.993.1 were in circulation and were made available to the relevant public before then. I understand that it is prior art to the Asserted Family 3 Patents.

366. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then G.993.1 renders obvious the asserted claims of the Family 3 patents when combined with other references as I explain below.

3. Claim 1 of the '048 Patent

367. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 1 of the '048 patent, as I describe below.

a. 1[a]. "A system that allocates shared memory"

368. To the extent that this preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory, in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55:65; col. 7:25-30; col. 8:58-9:3.

369. Fadavi-Ardekani discloses an ADSL system that includes an Interleave/De-Interleave Memory (IDIM) and a framer/coder/interleaver (FCI) that uses the IDIM for interleaving and deinterleaving. Fadavi-Ardekani, Abstract ("A transceiver for an asymmetric

communication system is provided that implements a buffering and scheduling scheme that uses a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions . . . . The FCI also interfaces a Digital Signal Processing (DSP) core through an Interleave/De-Interleave Memory (IDIM). . . . IDIM holds DMT frames of data and may also be utilized in a ping-pang fashion. . . . Memory is shared by multiple ADSL sessions and for the transmit and receive processes within an individual session."); *see also id.* at Fig. 2; col. 3:5-25. Fadavi-Ardekani explains that "'ping-pang' means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent," so that within a shared memory, "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." *Id*. at col. 5:60-65.

370. The FCI "supports multiple ADSL sessions," and performs functions including "Reed-Solomon encoding/decoding." *Id.* at col. 6:9-15. The FCI accesses the Interleave/De-Interleave Memory (IDIM), which "holds DMT frames of data and may be utilized in a ping-pang fashion . . . to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core." *Id.* at col. 6:55-60. Fadavi-Ardekani explains that "the DSP core may load new DMT frames of [receive] data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:62-65.

371. One of ordinary skill in the art would have understood the IDIM to be "shared memory." I understand that the Court has construed this term to mean "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." The IDIM of Fadavi-Ardekani meets this limitation because it "holds DMT frames

of data and may be utilized in a ping-pang fashion." *Id.* at col. 6:57-58. According to Fadavi-Ardekani, "'ping-pang' means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent." *Id.* at col. 5:60-65. When the memory is used in ping-pang fashion, "[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors." *Id.* at col. 5:65-6:1. A clock signal governs whether "an agent is allowed to access either a ping area of memory or a pang area of memory." *Id.* at col. 6:1-4. Thus, in my opinion, the IDIM described in Fadavi-Ardekani is a "shared memory."

372. Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions. *Id.* at col. 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path)."); col. 8:58-9:3 ("The IDIM may also be used in a ping-pang fashion by the FCI and the DSP core based on the virtual clock cycle. For example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX[receive] data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory. Between the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.").

373. Thus, it is my opinion that Fadavi-Ardekani discloses the preamble.

b. <u>1[b]. "a transceiver that is capable of"</u>

374. In my opinion, Fadavi-Ardekani discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. I understand that the Court has construed the term "transceiver" to mean "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry."

375. The central office ADSL transceiver of Fadavi-Ardekani is a communications device capable of transmitting and receiving data. Fadavi-Ardekani discloses "[a] transceiver for an asymmetric communication system . . . that implements a buffering and scheduling scheme that utilizes a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions." *Id.* at Abstract; *see also id.* at col. 2:62-67. The central office ADSL transceiver is described as being "bi-directionally coupled" to a splitter and a digital network. *Id.* at col. 4:30-34. It includes, as shown in FIG. 2 of Fadavi-Ardekani, an ATM accelerator, which, among other things, "transfers [] DMT tone data on the twisted-pair media." *Id.* at col. 5:52-54. FIG. 3 of Fadavi-Ardekani, shown above, "illustrates an exemplary processing sequencing for a case when four Transmit and Receive lines are enabled." *Id.* at col. 4:1-2. One of ordinary skill in the art would have understood these disclosures to indicate that the transceiver is capable of transmitting and receiving data.

376. Fadavi-Ardekani further teaches that the transmitter and receiver portions share common circuitry, including the Asynchronous Transfer Mode (ATM) accelerator, frame buffer, framer/coder/interleaver, DSP core and interleave/deinterleave memory (IDIM). *Id.* at col. 5:23-40; *see also id.* at FIG. 2.

377. G.993.1 similarly discloses a transceiver, a VTU-O or VTU-R that is compliant with the G.993.1 standard. *See* G.993.1, §§ 5.2, 5.3, Fig. 5-2. Accordingly, it is my opinion that Fadavi-Ardekani and G.993.1 disclose this limitation.

c. __1[c]. "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver"__

378. Fadavi-Ardekani in view of G.993.1 discloses limitation 1[c]. *See, e.g.*, G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

379. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

380. As explained above, the VDSL transceivers described in G.993.1 are capable of sending and receiving messages during initialization that specify communications parameters, including interleaver settings and capabilities. *See* G.993.1, § 12.4.1 ("Initialization of a VTU-O/VTU-R includes a variety of tasks. The set of tasks consists of: . . . exchange of parameters (RS settings, interleaver parameters, VOC settings, bit loading and energy tables . . . ."). Initialization messages include R-MSG2, sent by the VTU-R, which "transmits information about [the connection's] bit allocation capabilities and several other features," including the "Maximal interleaver memory," expressed in bytes. *Id.* at § 12.4.6.3.1.1; § 12.4.6.2.1.1 (Table 12-23). Thus, G.993.1 describes a transceiver, namely the VTU-R, transmitting a message during initialization (i.e., R-MSG2) specifying a maximum number of bytes of memory that are

available to be allocated to an interleaver (i.e., the VTU-R's interleaver). It also describes a transceiver, namely the VTU-O, receiving a message during initialization (i.e., R-MSG2) specifying the maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R's interleaver).

381. Similarly, G.993.1 specifies that the VTU-O transmits the message O-MSG2. *Id.* at § 12.4.6 (Figure 12-7). O-MSG2 contains the field "Maximum interleaver delay," expressed in milliseconds. *Id.* at § 12.4.6.2.1.1 (Table 12-23). As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, the interleaver delay is a function of the bit rate and interleaver depth. Therefore, G.993.1 discloses a transceiver, namely the VTU-O, transmitting a message during initialization (i.e., O-MSG2) that meets this limitation under TQ Delta's interpretation of the claims. It also discloses a transceiver, namely the VTU-R, receiving a message during initialization (i.e., O-MSG2) that meets this limitation under TQ Delta's interpretation of the claims.

d. 1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"

382. Fadavi-Ardekani discloses limitation 1[d], in my opinion. *See, e.g.* Fadavi-Ardekani, col. 6:55-65; col. 6:66-7:33; col. 8:58-9:3; col. 6:10:15.

383. First, Fadavi-Ardekani discloses that the FCI performs Reed-Solomon coding on the data to be transmitted and decoding on received data. Fadavi-Ardekani, col. 6:10-15 ("The FCI Supports multiple ADSL sessions and performs various tasks on payload data including: framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving."). Second, Fadavi-Ardekani discloses that "[a]ll functionalities of the FCI are provided as per ADSL standards," which include G.992.2 and T1.413 Issue 2. *Id.* at col. 6:19-

23. As a skilled artisan would have understood as of the Family 3 patents' priority date, G.992.2 and T1.413 Issue 2 specify Reed-Solomon encoding.

384. Fadavi-Ardekani also discloses that the DSP core uses the IDIM to transfer frames to and from the FCI, (*see, e.g.*, *id.* at col. 6:55-60), and that the IDIM is a shared memory. *See, e.g.*, *id.* at col. 6:57-58 ("The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion."); col. 5:60-6:4 ("'Ping-pang' means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent. As long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors. At any time, an agent is allowed to access either a ping area of memory or a pang area of memory based on the logic level of the virtual clock signal."); col. 8:58-9:3 ("The IDIM may also be used in a ping-pang fashion by the FCI and the DSP core based on the virtual clock cycle. For example, between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory. Between the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory.").

385. Fadavi-Ardekani further discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory. *See, e.g., id.* at col. 6:55-65 ("The Interleave/De-Interleave Memory

(IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core. In addition to interleave data storage, the IDIM may contain a dedicated area for the transfer of fast path data to the DSP Core. The IDIM may be organized as 16 bit words with byte write capability to allow beneficial performance of various interleave/de-interleave processes."); col. 6:66-7:33 ("In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention. The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing, for a total of 72 Kbytes for four sessions. A fast path buffer is also required for fast path data in both the interleave and de-interleave processes and requires 256 bytes of RAM per session, or a total of 1 K bytes for four sessions. Since the smallest RAM block currently available is 1 K×16, 1 K×16 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path).

An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path). With a lesser interleave depth, additional sessions may be supported with the same size buffer. With a larger buffer, additional session may be supported."); *see also* col. 8:58-9:3.

386. Thus, it is my opinion that Fadavi-Ardekani discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory.

e. <u>1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate"</u>

387. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses limitation 1[e]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; col. 6:10-15; G.993.1, §§ 8.4.1.

388. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. *See* Fadavi-Ardekani, col. 6:10-15. Fadavi-Ardekani also discloses that the FCI functions are in accordance with "ADSL standards," such as G.992.2 and T1.413 Issue 2 (*id.*at col. 6:19-23), and that the "ADSL transceiver of the invention may alternatively incorporate other variations of DSL," such as VDSL.

389. G.993.1 also discloses the transmitter interleaving the bytes of Reed-Solomon codewords. *See* G.993.1, § 8.4.1 ("Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255."). The depth of the interleaver in G.993.1 is

adjustable, to meet latency requirements. *Id.* With respect to the memory needed for an interleaver and a deinterleaver, G.993.1 notes that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver." *Id.*

390. Fadavi-Ardekani discloses allocating a first number of bytes of a shared memory to an interleaver. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where "[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent." *Id.* at col. 5:60-63; col. 6:57-60 ("The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core."). A portion of the memory is then allocated to an interleaver to interleave a first plurality of Reed Solomon coded data bytes, by determining the size of the memory needed to interleave a certain amount of data. *Id.* at col. 7:3-33. And as Fadavi-Ardekani notes, "between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory," and, similarly, "[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, these disclosures indicate that a first number of bytes of the shared memory have been allocated to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate.

391. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

f. <u>1[f]. "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"</u>

392. In my opinion, Fadavi-Ardekani in view of G.993.1 discloses limitation 1[f]. *See, e.g.*, G.993.1, §§ 8.4, 8.4.2, 12.4.1, 12.4.6.2.1.1.

393. I have reviewed TQ Delta's infringement contentions, and I understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, G.993.1 in combination with Fadavi-Ardekani still discloses this limitation in my opinion.

394. As explained above, G.993.1 describes a transceiver, namely the VTU-R, transmitting a message during initialization (i.e., R-MSG2) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R's interleaver). It also describes a transceiver, namely the VTU-O, receiving a message during initialization (i.e., R-MSG2) specifying the maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-R's interleaver). It also describes a transceiver, namely the VTU-O, transmitting a message during initialization (i.e., O-MSG2) specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (i.e., the VTU-O's interleaver) according to TQ Delta's infringement read. It also discloses a transceiver, namely the VTU-R, receiving a message (i.e., O-MSG2) during initialization specifying the maximum number of bytes of memory that are available to be

allocated to an interleaver (i.e., the VTU-O's interleaver) according to TQ Delta's infringement read.

395. Fadavi-Ardekani presents its disclosure in the context of G.992.2 and T1.413 Issue 2 but indicates that the transceiver may alternatively incorporate other variations of DSL, including VDSL, which a person having ordinary skill in the art as of the Family 3 patents' priority date would have understood would include G.993.1. *See, e.g.*, Fadavi-Ardekani at col. 4:18-21. Thus, a person having ordinary skill in the art would have understood that the transceiver of Fadavi-Ardekani could implement G.993.1, including its initialization protocol.

396. As explained above, Fadavi-Ardekani discloses a single transceiver supporting multiple sessions (lines). In allocating memory for each of the lines, Fadavi-Ardekani discloses determining the amount of memory necessary to support different sessions required by the transceiver. *See* Fadavi-Ardekani, col. 7:3-33. The transceiver of Fadavi-Ardekani is a central office transceiver that, if implementing G.993.1, would implement the functions of one or more VTU-Os. Thus, the interleaver of claim 1 of the '048 patent is the VTU-O's interleaver. As of the Family 3 patents' priority date, a person having ordinary skill in the art would have understood, based on the disclosures of Fadavi-Ardekani, that the allocated memory for the interleaver for each of the supported lines, which would have been determined based on the content of the O-MSG2 message transmitted by the VTU-O corresponding to that line, would not exceed the requirements the VTU-O set for itself in O-MSG2.

397. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

g. <u>1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"</u>

398. In my opinion, Fadavi-Ardekani in view of G.993.1 discloses limitation 1[g]. *See, e.g.*, Fadavi-Ardekani, col. 6:10-15; col. 5:57-6:6; col. 6:55-7:33; 8:58-9:3; G.993.1, § 8.4.1, 8.1.

399. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding and decoding, and interleaving and deinterleaving. *See* Fadavi-Ardekani, col. 6:10-15. G.993.1 also discloses the transmitter interleaving the bytes of Reed-Solomon codewords, which means that the receiver will need to deinterleave the bytes of the Reed-Solomon codewords to recover the transmitted data. *See* G.993.1, § 8.4.1 ("Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255."). The depth of the interleaver is adjustable, to meet latency requirements. *Id.* With respect to the memory needed for an interleaver and a deinterleaver, G.993.1 notes that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver." *Id.*

400. As explained above, the transceiver of Fadavi-Ardekani would be the VTU-O(s) of G.993.1 if it implemented VDSL. Fadavi-Ardekani discloses allocating a second number of bytes of a shared memory to a deinterleaver, which would then deinterleave data received from the VTU-R(s) connected to the transceiver of Fadavi-Ardekani. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where "[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent." *Id.* at col. 5:60-63; *see also id.* at col. 6:57-65 ("The IDIM holds DMT frames of data and may be utilized

in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core. In addition to interleave data storage, the IDIM may contain a dedicated area for the transfer of fast path data to the DSP Core. The IDIM may be organized as 16 bit words with byte write capability to allow beneficial performance of various interleave/de-interleave processes."). Thus, a portion of the memory is allocated to a deinterleaver to deinterleave a first plurality of Reed Solomon coded data bytes, by determining the size of the memory needed to deinterleave a certain amount of data. *See, e.g.*, *id.* at col. 7:3-33. And as Fadavi-Ardekani notes, "between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory," and, similarly, "[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, these disclosures indicate that a first number of bytes of the shared memory have been allocated to the deinterleaver to deinterleave a second plurality of Reed Solomon (RS) coded data bytes received at a second data rate.

h. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

401. It is my opinion that Fadavi-Ardekani and G.993.1 together disclose limitation 1[h]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 7:25-30; col. 8:58-9:3; G.993.1 at §§ 8.1, 8.4.1, Fig. 8-1.

402. G.993.1 discloses the VTU-O interleaving the first plurality of RS coded data bytes, and deinterleaving the second plurality of RS coded data bytes. *See* § 8.4.1 ("The same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver."); § 8.4.2.

403. As explained above, the transceiver of Fadavi-Ardekani would be the VTU-O(s) of G.993.1 if it implemented VDSL. Fadavi-Ardekani discloses interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver (i.e., prior to transmission to the VTU-R) and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver (i.e., after reception from the VTU-R). Fadavi-Ardekani discloses that "[a]n optimal implementation of the interleaver according to the method of the invention uses the same memory for receive data and transmit data . . ." Fadavi-Ardekani, col. 7:25-30. Fadavi-Ardekani further describes that the IDIM memory is used in a ping-pang fashion, in which "the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:58-9:3. And as Fadavi-Ardekani notes, "between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory," and, similarly, "[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, these disclosures indicate that the

transceiver of Fadavi-Ardekani, acting as one or more VTU-Os, is interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

i. <u>1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"</u>

404. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses limitation 1[i]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6, col. 6:55-65; col. 6:66-7:33; G.993.1, §§ 9.2.3.4.

405. I understand that the Court has construed this limitation to mean "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a "ping-pang" fashion, where "areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of a memory is being used by a first agent, another area of memory can be used by a different agent." Fadavi-Ardekani, col. 6:55-65. It further explains how "[a]s long as different agents access . . . different areas of a dual access memory, there are no memory address conflicts that could cause communication errors." *Id.* at col. 5:65-67. Fadavi-Ardekani explains that "[a]n optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4K fast path)." *Id.* at col. 7:25-30. Fadavi-Ardekani discloses that the shared

memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. Specifically, Fadavi-Ardekani discloses that "between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory," and, similarly, "[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:60-9:3. As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, these disclosures indicate that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

406. Additionally, G.993.1 discloses that the interleaver memory and the deinterleaver memory are used at the same time, which G.993.1 refers to as Frequency Division Duplexing (FDD). G.993.1, § 6.1. In this mode, a "full-duplex" link is established between the VTU-O and VTU-R, over which data can be transmitted simultaneously in both directions. *Id.* at §§ 12.4.1, 9.2.3.4. One of ordinary skill in the art would have understood that the VTU-O would need to interleave and deinterleave data at the same time in this mode of transmission.

407. Therefore, it is my opinion that claim 1 of the '048 patent is obvious over the combination of Fadavi-Ardekani and G.993.1.

4. <u>Claim 5 of the '381 Patent</u>

408. It is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 5 of the '381 patent.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

409. To the extent it is limiting, it is my opinion that Fadavi-Ardekani discloses the preamble. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; col. 7:34-43.

410. Fadavi-Ardekani describes how "the firmware required for performing processing tasks associated with the central office is resident on the single integrated circuit transceiver of the invention." *Id.* at col. 7:34-37. Though Fadavi-Ardekani notes that functions implemented in hardware are generally faster, "similar functionality can be provided in a software implementation." *Id.* at col. 7:37-43. I discuss how Fadavi-Ardekani discloses allocating shared memory in a transceiver above with respect to claim 1 of the '048 patent, which I incorporate here by reference. *See* Section IX.C.3.a. I describe how Fadavi-Ardekani discloses a transceiver above at Section IX.C.3.b, which I also incorporate by reference. Thus, Fadavi-Ardekani discloses this limitation.

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

411. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[b]. *See, e.g.*, G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.2.1.2, 12.4.6.3.1.1.

412. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or

other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

413. Above at Section IX.D.2.c, I describe how Fadavi-Ardekani in combination with G.993.1 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to a deinterleaver according to TQ Delta's apparent interpretation of the claims, and I incorporate that discussion by reference. Furthermore, G.993.1 discloses that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and deinterleaving at the receiver. The convolutional interleaving introduces an absolute read-to-write delay . . . ." G.993.1, § 8.4.1. Moreover, G.993.1 describes the similarities between the interleaver processing and the deinterleaver processing, stating that "[t]he deinterleaver is similar to the interleaver, but the branch indices are reversed so that the largest interleaver delay corresponds to the smallest deinterleaver delay." *Id.* at § 8.4.2, Table 8-1 (describing relationship between interleaver block depth, interleaving depth, "(De)interleaver memory size," and end-to-end delay). One of ordinary skill in the art would have understood that the discussions of allocating memory to an interleaver in Fadavi-Ardekani and G.993.1 apply equally to allocating memory to a deinterleaver. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

c. <u>5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"</u>

414. Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; 6:55-7:33; col. 8:58-9:3.

415. Above at Section 381, I describe how Fadavi-Ardekani in combination with G.993.1 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my discussion and opinions by reference. G.993.1 discloses the complementary relationship between the memory required by an interleaver and a deinterleaver, as I described above with respect to the previous limitation. *See* G.993.1, §§ 8.4.1, 8.4.2, Table 8-1. A person having ordinary skill in the art would have understood the disclosures of G.993.1 and Fadavi-Ardekani as disclosing that the transceiver determines an amount of memory required by the deinterleaver to deinterleaver a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. 5[d]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"

416. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, FIG. 8-1.

417. Above at Section IX.C.3.e, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate. In addition, at Section IX.C.3.g above, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of those discussions by reference, and on

that basis, it is my opinion that Fadavi-Ardekani in combination with G.993.1 discloses this limitation.

e. <u>5[e]. "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"</u>

418. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[e]. *See, e.g.*, G.993.1, §§ 8.4, 8.4.2, 12.4.1, 12.4.6.2.1.1. I have reviewed TQ Delta's infringement contentions, and understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. *See* G.993.2 (12/2011) at § 6.2.8. I do not agree with TQ Delta's contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, the combination of Fadavi-Ardekani and G.993.1 discloses this limitation, in my opinion.

419. Above at Section IX.C.3.f, I explain how Fadavi-Ardekani in combination with G.993.1 discloses "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message," and I incorporate that discussion by reference. In the same way that the CO transceiver of Fadavi-Ardekani and G.993.1 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, it would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

f. <u>5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"</u>

420. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses limitation 5[f]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, Fig. 8-1.

421. Above at Section IX.C.3.g, I explain how Fadavi-Ardekani allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also, at Section IX.C.3.e above, I explain how Fadavi-Ardekani in combination with G.993.1 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference. It is my opinion that, given this disclosure, Fadavi-Ardekani and G.993.1 disclose this limitation.

g. <u>5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"</u>

422. Fadavi-Ardekani in combination with G.993.1, in my opinion, discloses limitation 5[g]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 7:25-30; col. 8:58-9:3; G.993.1, §§ 8.1, 8.4.1, Fig. 8-1. Above at Section IX.C.3.h, I explain how Fadavi-Ardekani in combination with G.993.1 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a

transceiver would implement this limitation. It is my opinion that Fadavi-Ardekani and G.993.1 disclose this limitation.

h. 5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"

423. Fadavi-Ardekani in combination with G.993.1 discloses that the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.993.1, §§ 6.1, 9.2.3.4, 12.4.1. I explain above at Section IX.C.3.i how it is my opinion that Fadavi-Ardekani in view of G.993.1 discloses wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference between these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by Fadavi-Ardekani in combination with G.993.1.

5. Claim 13 of the '882 patent

424. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. 13[a]. "A system that allocates shared memory"

425. To the extent that the preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3. This limitation is identical to the preamble of Claim 1 of the '048 patent, and for the same reasons, it is my opinion that this limitation is disclosed by Fadavi-Ardekani. *See* Section IX.C.3.a.

b. <u>13[b]. "a transceiver that performs"</u>

426. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. This limitation is identical to the second limitation of Claim 1 of the '048 patent, except that it recites "a transceiver capable of" additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.C.3.b, and I incorporate my discussion and opinions herein by reference.

c. <u>13[c] through 13[i]</u>

427. These limitations are identical to the corresponding limitations of claim 5 of the '381 patent. *See* Appx. 3 (comparing limitations of claim 5 of the '381 patent with limitations of claim 13 of the '882 patent). For the same reasons, it is my opinion that these limitations are met by Fadavi-Ardekani in combination with G.993.1, and I incorporate by reference Sections IX.C.3.c through IX.C.3.i (claim 1) and Sections IX.B.4.b through IX.B.4.h (claim 5).

6. <u>Claim 19 of the '473 Patent</u>

428. In my opinion, Fadavi-Ardekani in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent.

a. <u>19[a]. "An apparatus comprising"</u>

429. To the extent that this preamble is limiting, Fadavi-Ardekani discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, Fadavi-Ardekani at Abstract; col. 1:12-14; col. 2:18-24; col. 2:62-67.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

430. It is my opinion that Fadavi-Ardekani discloses a multicarrier communications transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 1:12-14; col. 2:18-24; col. 2:62-67; G.993.1, §§ 5.2, 5.3, Fig. 5-2. I understand that the Court has construed the term "transceiver"

to mean "communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry."

431. The central office ADSL transceiver of Fadavi-Ardekani is a communications device capable of transmitting and receiving data. Fadavi-Ardekani discloses "[a] transceiver for an asymmetric communication system . . . that implements a buffering and scheduling scheme that utilizes a virtual clock signal to synchronize processing of asynchronous frame data for multiple ADSL sessions." *Id.* at Abstract; *see also id.* at col. 2:62-67. The central office ADSL transceiver is described as being "bi-directionally coupled" to a splitter and a digital network. *Id.* at col. 4:30-34. It includes, as shown in FIG. 2 of Fadavi-Ardekani, an ATM accelerator, which, among other things, "transfers [] DMT done data on the twisted-pair media." *Id.* at col. 5:52-54. FIG. 3 of Fadavi-Ardekani, shown above, "illustrates an exemplary processing sequencing for a case when four Transmit and Receive lines are enabled." *Id.* at col. 4:1-2. One of ordinary skill in the art would have understood these disclosures to indicate that the transceiver is capable of transmitting and receiving data.

432. Fadavi-Ardekani further discloses using a "conventional ADSL transceiver." *Id.* at col. 4:35-38. One of ordinary skill in the art would have understood that ADSL is a multicarrier communications system. Moreover, Fadavi-Ardekani discloses that ADSL uses "Discrete MultiTone (DMT), [which] is a multi-carrier technique that divides the available bandwidth of twisted-pair media connections into mini-subchannels or bins. In the ADSL standard, DMT may be used to generate up to 250 separate 4.3125 KHz subchannels from 26 KHz to 1.1 MHz for downstream transmission and up to 26 subchannels from 26 KHz to 138 KHz for upstream transmission." *Id.* at col. 2:3-9.

433. Fadavi-Ardekani further teaches that the transmitter and receiver portions share common circuitry, including the Asynchronous Transfer Mode (ATM) accelerator, frame buffer, framer/coder/interleaver, DSP core and interleave/deinterleave memory (IDIM). *Id.* at col. 5:23-40.

434. G.993.1 similarly discloses a multicarrier communications transceiver, a VTU-O or VTU-R that is compliant with the G.993.1 standard and uses DMT. *See* G.993.1, §§ 5.2, 5.3, 8.5.1, Fig. 5-2. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

c. <u>19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"</u>

435. Fadavi-Ardekani discloses limitation 1[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 6:66-7:33.

436. Fadavi-Ardekani discloses ADSL transceivers that include framer/coder/interleaver (FCI) blocks that perform interleaving and deinterleaving functions, and are associated with an Interleave/De-Interleave Memory (IDIM). *Id.* at col. 6:10-15. The IDIM is associated with multiple "sessions," where, for example, "a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2Kbytes for upstream processing." *Id.* at col. 13-17. I understand that the Court has construed the term "latency path" to mean "transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay." One of ordinary skill in the art would have understood the sessions of Fadavi-Ardekani to take place over multiple latency paths, and that a session requiring "downstream processing" requires interleaving, and a session requiring upstream processing requires deinterleaving. These latency paths would have distinct latencies.

437. Similarly G.993.1 discloses at least one upstream path and one downstream path between a VDSL VTU-O and VTU-R, with each of these paths being associated with a latency. *See* G.993.1, § 5.1 ("The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies."), § 5.2. One of ordinary skill in the art would have understood that these upstream and downstream paths are associated with interleaving and deinterleaving functions. *See, e.g.*, § 8.4.1 ("Interleaving shall be used to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. . . . It shall be possible to adjust the interleave depth via the management system to meet latency requirements. The latency of the slow path is a function of the data rate and burst error correction capability. For data rates greater than or equal to 13 Mbit/s, the latency between the α and β interfaces shall not exceed 10 ms when the interleaver depth is set to the maximum. At lower data rates there is a trade-off between higher latency and decreased burst error correction ability. At any data rate, the minimum latency occurs when the interleaver is turned off.").

438. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

d. <u>19[d]. "the multicarrier communications transceiver being associated with a memory"</u>

439. In my opinion, the combination of Fadavi-Ardekani and G.993.1 discloses limitation 19[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.993.1 at § 8.4.1, Table 8-1, Table 8-2.

440. Fadavi-Ardekani describes an Interleave/De-interleave Memory (IDIM), which is associated with the transceiver. Fadavi-Ardekani, col. 6:55-65 ("The Interleave/De-Interleave Memory (IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion."); col. 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 kBytes to support a standard ADSL session at full interleave depth (16K interleave & deinterleave +4K fast path)."); *see also* Fadavi-Ardekani, col. 8:58-9:3.

441. Fadavi-Ardekani further describes that the "ADSL transceiver of the invention 120 is a single integrated circuit which has various component[s] including: an Asynchronous Transfer Mode (ATM) accelerator 222, a Frame Buffer (FB) 224, a Framer/Coder/Interleaver (FCI) 226, a Digital Signal Processing (DSP) core 228, and a Interleave/De-Interleave Memory (IDIM) 230." *Id.* at col. 5:23-28. Because the IDIM is described and disclosed as being part of the ADSL transceiver, one of ordinary skill in the art would have understood it to be "associated with" the transceiver.

442. G.993.1 also discloses that the multicarrier communications transceiver is associated with a memory. *See, e.g.*, G.993.1 at § 8.4.1 ("The convolutional interleaver uses a memory in which a block of I octets is written while an (interleaved) block of I octets is read. . . . The same size interleaving memory (see Table 8-1) is needed for interleaving at the

transmitter and de-interleaving at the receiver."); *see also* Table 8-1 (indicating interleaver and deinterleaver memory size is (M – 1)x(I – 1)/2 bytes); Table 8-2 (providing interleaver and deinterleaver memory sizes for a particular Reed-Solomon code).

443. Therefore, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

e. 19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

444. Fadavi-Ardekani, in combination with G.993.1, discloses limitation 19[e], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

445. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.993.1 in combination with Fadavi-Ardekani discloses this limitation under TQ Delta's interpretation of the claims.

446. Fadavi-Ardekani discloses allocating memory between an interleaving function and a deinterleaving function. Fadavi-Ardekani describes using the IDIM memory in a ping-pang fashion, where "[a]s one area of the memory is being used by a first agent, another area of the memory can be used by a different agent." *Id.* at col. 5:60-63; col. 6:57-60 ("The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames the FCI core and the DSP core.").

A portion of the memory is allocated to an interleaver by determining the size of the memory needed to interleave a certain amount of data. *Id.* at col. 7:3-33. And as Fadavi-Ardekani notes, "between the events of the virtual clock signal transition and the rising edge of the TX processes are complete signal (TX_Complete 324), the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory," and, similarly, "[b]etween the events of TX_Complete 324 and signal that all RX processes are complete (RX_Complete 328), the DSP core can read TX data from the portion of the IDIM used as interleave memory while FCI is accessing the portion of the IDIM used as de-interleave memory." *Id.* at col. 8:60-9:3. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function." As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, these disclosures indicate that the memory is allocated between an interleaving function and a deinterleaving function.

447. As explained above, VDSL transceivers described in G.993.1 are capable of sending messages during initialization, specifying communications parameters, including interleaver and deinterleaver settings and capabilities. G.993.1 discloses transceivers that exchange initialization messages. *See* G.993.1, § 12.4.1 ("Initialization of a VTU-O/VTU-R includes a variety of tasks. The set of tasks consists of: . . . exchange of parameters (RS settings, interleaver parameters, VOC settings, bit loading and energy tables . . . ."). Initialization messages include R-MSG2, sent by the VTU-R, that "transmits information about [the connection's] bit allocation capabilities and several other features," including the "Maximal

interleaver memory," expressed in bytes. *Id.* at § 12.4.6.3.1.1; § 12.4.6.2.1.1 (Table 12-23). Thus, G.993.1 describes a message during initialization (i.e., R-MSG2) that describes how interleaver memory can be allocated to an interleaver or a deinterleaver. It also describes how a VTU-O receives a message during initialization (i.e., R-MSG2) specifying parameters based on which the memory can be allocated (i.e., the VTU-R's interleaver).

448. Similarly, G.993.1 specifies that the VTU-O transmits the message O-MSG2. *Id.* at § 12.4.6 (Figure 12-7). O-MSG2 contains the field "Maximum interleaver delay," expressed in milliseconds. *Id.* at § 12.4.6.2.1.1 (Table 12-23). As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, because the interleaver delay is a function of the bit rate and interleaver depth, O-MSG2 specifies parameters that the VTU-O can use to allocate memory between an interleaver and a deinterleaver. It also discloses a transceiver, namely the VTU-R, receiving a message during initialization (i.e., O-MSG2) that the transceiver can use to allocate memory between an interleaver and a deinterleaver (i.e., the VTU-O's interleaver).

f. <u>19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"</u>

449. Fadavi-Ardekani, in combination with G.993.1, discloses limitation 19[f], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 8:58-9:3; G.993.1, §§ 8.4.1, 8.4.2.

450. As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a "ping-pang" fashion used by multiple functions, where "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." Fadavi-Ardekani, col. 6:60-65. In operation, the shared memory disclosed in Fadavi-Ardekani

in which "the DSP core may load new DMT frames of RX data to a portion of the IDIM used as de-interleave memory while the FCI is using a portion of the IDIM as interleave memory." *Id.* at col. 8:58-9:3. The allocation of memory is based on the number of sessions supported by the transceiver and the interleave depth for each session. *See, e.g.*, *id.* at col. 7:3-33.

451. As I explain above (*see* Section VII.F.4), G.993.1 discloses that the VTU-O and VTU-R exchange interleaver capabilities and requirements during initialization. Fadavi-Ardekani states that its transceiver may incorporate VDSL. Fadavi-Ardekani at col. 4:18-21. Thus, as a skilled artisan would have recognized as of the priority date of the Family 3 patents, the transceiver of Fadavi-Ardekani implementing VDSL as per G.993.1 would transmit and receive initialization messages regarding interleaving capabilities and requirements. Thus, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

452. Additionally, G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. G.993.1 uses Frequency Division Duplexing (FDD). G.993.1, § 6.1. In this mode, a "full-duplex" link is established between the VTU-O and VTU-R, over which data can be transmitted simultaneously in both directions. *Id.* at §§ 12.4.1, 9.2.3.4. One of ordinary skill in the art would have understood that data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function.

453. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 discloses this limitation.

7. <u>Motivation to Combine Fadavi-Ardekani and G.993.1</u>

454. In my opinion, one of ordinary skill in the art as of the Family 3 patents' priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 in the manner claimed.

455. First, both references are in the telecommunications field and relate to DSL systems specifically. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:63-3:4; col. 4:9-21; col. 4-25:63 (describing an ADSL communication system); col. 4:65-5:40 (describing head-end ADSL transceiver); G.993.1, §§ 1 ("G.993.1 VDSL (Very high speed Digital Subscriber Line) permits the transmission of asymmetric and symmetric aggregate data rates up to tend of Mbit/s on twisted pairs."). In addition, Fadavi-Ardekani states that the disclosed transceiver may implement VDSL, which, as of the Family 3 patents' priority date, would have been understood by one of ordinary skill in the art to include G.993.1. *See, e.g.*, Fadavi-Ardekani, col. 4:18-21. For this reason alone, a skilled artisan would have been motivated to combine the teachings of G.993.1 with those of Fadavi-Ardekani.

456. Second, both references describe the need to allocate memory for interleaving and deinterleaving functions. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3, G.993.1 at § 8.4.1 (describing implementation of interleaver memory, and noting that "[t]he same size interleaving memory (see Table 8-1) is needed for interleaving at the transmitter and de-interleaving at the receiver."). Thus, both Fadavi-Ardekani and G.993.1 relate to the problem to be solved identified by the Family 3 patents – allocating shared memory between interleaving and deinterleaving functions. *See, e.g.*, '048 patent, col. 1:48-59 ("One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to

provide error correcting capability."). One of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions when considering G.993.1 and its description of using interleavers and exchanging parameters relating to interleaving during initialization.

457. Third, as a skilled artisan would have understood on the Family 3 patents' priority date, the memory requirements of VDSL transceivers, such as those described in G.993.1, contributed to the transceiver's cost, power consumption, and size. The need to reduce size and power was known to be particularly acute for VDSL transceviers because the VTU-O was to be deployed in optical network units or cabinets, in which space was at a premium and heat dissipation mechanisms were limited. Thus, a skilled artisan would have sought implementations that would reduce the cost, size, and power consumption of the VTU-O. Fadavi-Ardekani discloses reducing the size and complexity of memory in a DSL transceiver. *See, e.g.*, Fadavi-Ardekani, col. 3:1-4 ("Utilizing this buffering and scheduling methodology, reductions in the design sizes of various transceiver components and the data flow complexity of the transceiver may be achieved."). Fadavi-Ardekani faults prior art systems for being "excessively duplicative in terms of transceivers and memory in each transceiver, and thus more costly than necessary to provide the desired functionality." *Id.* at col. 2:57-59. It also discloses the desirability of reducing the amount of memory needed. *Id.* at col. 3:43-47; col. 8:4-12; 9:20-23. To reduce memory, Fadavi-Ardekani discloses sharing one memory between the interleaver and deinterleaver. *See, e.g., id.* at Abstract; col. 3:39-41; col. 7:25-30; col. 9:18-20. Thus, a skilled artisan would have been motivated to combine the size- and cost-saving

approach of Fadavi-Ardekani with the transceivers of G.993.1 to reduce the cost, size, and power consumption of the VTU-Os that would be deployed in optical network units or cabinets.

458. Fourth, one of ordinary skill in the art, when considering Fadavi-Ardekani, would have naturally looked to G.993.1 to determine how to allocate shared memory. Fadavi-Ardekani explains that the amount of memory required by, and the allocation of memory between, the interleaver and deinterleaver depends on the services to be supported. Fadavi-Ardekani, col. 6:66-7:33 ("In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention."). One of ordinary skill would have recognized that, in order to allocate memory between interleaver and deinterleaver functions in a useful way, the transceiver would need information about the amount of memory needed for the services that were to be supported by the transceiver.

459. As I described above, G.993.1 discloses that the transceivers share information about the services they will support, the latency requirements of those services, and the amount of available memory. *See, e.g.*, G.993.1, § 5.1 ("The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and upstream data paths. A single path in each direction can be of high latency (with low BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and other

requesting more than two paths/latencies. The model assumes that Forward Error Correction (FEC) will be needed for part of the payload and that deep interleaving will be required to provide adequate protection against impulse noise."); § 8.5.2; § 12.4.6.2, § 12.4.6.3; Table I.39. One of ordinary skill in the art would have recognized that G.993.1, and the ability of transceivers to share information about their capabilities and requirements during the initialization procedure, provides a reliable and efficient way of implementing the advantageous single memory for interleaving and deinterleaving disclosed by Fadavi-Ardekani for a wide variety of services and applications such as those enabled by G.993.1.

D. The Asserted Claims Are Obvious Over Fadavi-Ardekani in Combination with G.992.2

460. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent. One of ordinary skill in the art would have been motivated, as of the Family 3 patents' priority date, to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2, as I describe below in Section IX.D.6. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Fadavi-Ardekani in combination with G.992.2 renders obvious the asserted claims of the Family 3 patents.

1. Brief Description of G.992.2

461. I provide a description of G.992.2 above at Section VII.F.3, which I incorporate herein by reference.

462. I understand that G.992.2 was approved and published no later than June 1999. I understand that it is prior art to the Asserted Family 3 Patents. I have reviewed TQ Delta's

infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then G.992.2 renders obvious the asserted claims of the Family 3 patents when combined with other references as I explain below.

2. <u>Claim 1 of the '048 Patent</u>

463. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 1 of the '048 patent, as I describe below.

a. <u>1[a]. "A system that allocates shared memory"</u>

464. To the extent that this preamble is limiting, Fadavi-Ardekani discloses a system that allocates shared memory, in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55:65; col. 7:25-30; col. 8:58-9:3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.a.

b. <u>[1b]. "a transceiver that is capable of"</u>

465. In my opinion, Fadavi-Ardekani discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; G.992.2, §§ 4.1, 4.2, 5, Fig. 2. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.b.

466. G.992.2 similarly discloses a transceiver, an ADSL transceiver unit (ATU) that complies with the G.992.2 standard. *See* G.992.2, §§ 4.1, 4.2, Fig. 2. G.992.2 explains that "[t]he ATU shall transport a single duplex bearer channel," which would indicate to one of ordinary skill in the art that the ATU is capable of transmitting and receiving data. One of ordinary skill in the art would further have understood that the transmitter and receiver portions share some common circuitry, such as, for example, an interface to the twisted pair.

c. <u>1[c] "transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to allocated to an interleaver"</u>

467. Fadavi-Ardekani in view of G.992.2 discloses limitation 1[c], in my opinion. *See, e.g.*, G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

468. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, nor do I agree with TQ Delta's infringement read. If, however, the Court or other trier of fact interprets the claim such that the O-PMS message and sending max_delay_octet meets this limitation, then Fadavi-Ardekani and G.992.2 meet this limitation as well, in my opinion.

469. Transceivers such as those described in G.992.2 are capable of sending and receiving initialization messages that specify communication parameters for DSL systems. For example, G.992.2 teaches transceivers that exchange initialization messages that contain information about the channel as well as the transceiver and its processing requirements and capabilities. G.992.2, § 11.1.1 ("In subsequent parts of the initialization, in order to maximize the throughput and reliability of this link, ADSL transceivers shall determine certain relevant attributes of the connecting channel and establish transmission and processing characteristics suitable to that channel. During initialization each receiver can determine the relevant attributes of the channel through the transceiver training and channel analysis procedures."). These messages include communicating to a far-end transceiver "the number of bits and relative power levels to be used on each DMT subcarrier, as well as any messages and final data rates information." *Id.*

470. G.992.2 describes exchanging messages between the transceivers in an iterative process to establish transmission parameters such as data rates and formats for the ATU-R. The C-RATES1 message defined in G.992.2 is a signal sent from the ATU-C, whose purpose "is to transmit four options for data rates and formats to the ATU-R." *Id.* at § 11.9.2. Each of the four options contains three fields, one of which is the RRSI field that "contains Reed-Solomon FEC and interleaver parameters." The RRSI field contains ten entries, including the number of data frames (DFs) per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleaver depth in codewords. *See id.*; *see also* Table 26, Table 27. One of ordinary skill in the art would have understood that these messages would meet this claim limitation, at least according to TQ Delta's infringement read.

471. An additional initialization message is the C-RATES-RA message, which sends "four new options for transport configuration for both upstream and downstream. These options will, in general, be closer to the optimum bit rate for the channel than those in C-RATES1. . . ." G.992.2, § 11.11.3. Like the C-RATES1 message, the C-RATES-RA message contains ten entries, including the numbers of DFs per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleave depth in codewords. *See id.*; *see also* Table 33, Table 34. As with the parameters in the C-RATES1 message, one of ordinary skill in the art would have understood that the information in the C-RATES-RA message would meet this limitation under TQ Delta's interpretation of the claim.

472. In addition, the ATU-R transmits R-RATES2, which selects the number of the option in C-RATES-RA with the highest data rate that can be supported in the downstream

direction based on the ATU-R's measurements of the channel. G.992.2 at § 11.12.10. The ATU-C then transmits C-RATES2, which indicates the final decision on the downstream and upstream options that will be used for the connection. G.992.2 at § 11.11.11. The ATU-C's decision combines the downstream option selected by the ATU-R with the option number with the highest upstream data rate that can be supported based on the ATU-C's measurements of the channel. G.992.2 at § 11.11.11. A person having ordinary skill in the art would have understood that the information in the R-RATES2 and C-RATES2 messages meets this limitation, at least under TQ Delta's infringement read.

d. <u>1[d]. "determining an amount of memory required by the interleaver to interleave a first plurality of Reed-Solomon (RS) coded data bytes within the shared memory"</u>

473. Fadavi-Ardekani in combination with G.992.2. discloses limitation 1[d], in my opinion. *See, e.g.* Fadavi-Ardekani, col. 6:55-65; col. 6:66-7:33; 8:58-9:3; 6:10:15; G.992.2, § 7.6. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section 381.

e. <u>1[e]. "allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first rate"</u>

474. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses limitation 1[e]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; col. 6:10-15; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

475. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. *See* Fadavi-Ardekani, col. 6:10-15. G.992.2 also discloses interleaving the bytes of Reed-Solomon codewords. *See* G.992.2, § 7.6 ("The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2."). The depth of the interleaver is adjustable, to meet different data rates and demands. *Id.*

476. As I explained above, Fadavi-Ardekani discloses allocating a first number of bytes of a shared memory to an interleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.e. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

f. 1[f]. "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"

477. In my opinion, Fadavi-Ardekani in view of G.992.2 discloses limitation 1[f]. *See, e.g.*, G.992.2, §§, 7.6, 11.1.1, 11.9.2, 11.11.3.

478. I have reviewed TQ Delta's infringement contentions, and I understand that TQ Delta contends that the "maximum number of bytes specified in the message" is met by the aggregate interleaver delay parameter and the O-PMS message. *See* G.993.2 (12/2011) at §§ 6.2.8; 12.3.5.2.1.3. I do not agree with TQ Delta's contentions or interpretation of the claims. To the extent that the Court or the trier of fact interprets the claim consistent with TQ Delta's contentions, however, G.992.2 in combination with Fadavi-Ardekani still discloses this limitation in my opinion.

479. First, one of ordinary skill in the art would have understood, given the disclosure of Fadavi-Ardekani, that the allocated memory for the interleaver would not exceed the requirements set forth by the transmitter. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.f.

480. Second, G.992.2 discloses the C-RATES1, R-RATES1, C-RATES-RA, R-RATES2, and C-RATES2 messages, which contain the RRSI field that contains values for the number of DFs in a Reed-Solomon codeword, and the interleaver depth in codewords in the upstream and downstream directions. *See, e.g.*, G.992.2, §§ 11.9.2, 11.11.3. G.992.2 also discloses that the interleaver depth is adjustable. *Id.* at § 7.6. The parameters in the C-

RATES1, R-RATES1, and C-RATES-RA messages can be used to allocate memory to implement each of the four options. The R-RATES2 and C-RATES2 messages can be used to allocate memory to implement the ATU-C's interleaver and to implement the ATU-R's interleaver. Based on this disclosure, one of ordinary skill in the art would have understood that the memory allocated for the interleaver does not exceed the number of bytes in the message.

g. 1[g]. "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

481. In my opinion, Fadavi-Ardekani in view of G.992.2 discloses limitation 1[g]. *See, e.g.*, Fadavi-Ardekani, col. 6:10-15; col. 5:57-6:6; col. 6:55-7:33; 8:58-9:3; G.992.2, §§7.6, 11.1.1, 11.9.3.

482. As described above, Fadavi-Ardekani discloses the use of Reed-Solomon encoding. *See, e.g.*, Fadavi-Ardekani, col. 6:10-15. G.992.2 also discloses interleaving the bytes of Reed-Solomon codewords. *See* G.992.2, § 7.6 ("The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2" and describing a rule for interleaver depth). The depth of the interleaver is adjustable, to meet different service requirements. *See id.* As a skilled artisan would have understood, the specification in G.992.2 that Reed-Solomon codewords shall be convolutionally interleaved by a transmitter means that the transceiver on the other side of the subscriber line would include a corresponding deinterleaver.

483. Fadavi-Ardekani discloses allocating a second number of bytes of a shared memory to a deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.g. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

h. 1[h]. "interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver"

484. It is my opinion that Fadavi-Ardekani and G.992.2 together disclose limitation 1[h]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.3.

485. One of ordinary skill in the art would have understood that G.992.2 discloses interleaving a first plurality of RS coded data bytes, and deinterleaving a second plurality of RS coded data bytes. *See* § 7.6 ("The Reed-Solomon codewords shall be convolutionally interleaved. The interleaving depth shall always be a power of 2."). Given G.992.2's disclosure of a convolutional interleaver, and that each ATU supports both downstream and upstream transmission simultaneously (*see, e.g.*, G.992.2 at §§ 4.2, 7.3, 7.10), one of ordinary skill in the art would have understood that an ATU would interleave data bytes to be transmitted and deinterleave received data bytes.

486. Fadavi-Ardekani discloses interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.h. It is my opinion that Fadavi-Ardekani and G.992.2 disclose this limitation.

i. 1[i]. "wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver"

487. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses limitation 1[i]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6, col. 6:55-65; col. 6:66-7:33; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

488. As described above, Fadavi-Ardekani discloses that the shared IDIM memory operates in a "ping-pang" fashion in which the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.3.i.

489. Additionally, one of ordinary skill would have understood that G.992.2 discloses that the interleaver memory and the deinterleaver memory are used at the same time. G.992.2 establishes a "single duplex bearer channel." G.992.2, § 5. One of ordinary skill in the art would have understood that data is transmitted in both directions at the same time. As a result, the interleaver and deinterleaver would both have to be used at the same time, which in turn, would mean that the interleaver memory and deinterleaver memory were used at the same time. Accordingly, it is my opinion that G.992.2 also discloses this limitation.

3. Claim 5 of the '381 Patent

490. It is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 5 of the '381 patent.

a. 5[a]. "A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

491. To the extent that it is limiting, it is my opinion that Fadavi-Ardekani discloses the preamble. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; col. 7:34-43.

492. Fadavi-Ardekani describes how "the firmware required for performing processing tasks associated with the central office is resident on the single integrated circuit transceiver of the invention." *Id.* at col. 7:34-37. Though Fadavi-Ardekani notes that functions

implemented in hardware are generally faster, "similar functionality can be provided in a software implementation." *Id.* at col. 7:37-43. I discuss how Fadavi-Ardekani discloses allocating shared memory in a transceiver above with respect to claim 1 of the '048 patent, which I incorporate here by reference. *See* Section IX.C.3.a. I describe how Fadavi-Ardekani discloses a transceiver above at Section IX.C.3.b, which I also incorporate by reference. Thus, Fadavi-Ardekani discloses this limitation.

b. 5[b]. "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver"

493. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[b]. *See, e.g.*, G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3.

494. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by sending or receiving the O-PMS message described in VDSL2. I do not agree that sending or receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then G.992.2 and Fadavi-Ardekani disclose this limitation under such an interpretation of the claims.

495. Above at Section IX.D.2.c, I describe how Fadavi-Ardekani in combination with G.992.2 discloses transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to allocated to a deinterleaver, and I incorporate that discussion by reference. Furthermore, G.992.2 describes the relationship between the interleave depth of a convolutional interleaver and the memory required to interleave or deinterleave a certain amount of data. *See* G.992.2, § 7.6.

Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation under TQ Delta's interpretation of the claims.

c. 5[c]. "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory"

496. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; 6:55-7:33; col. 8:58-9:3.

497. Above at Section IX.D.2.d, I describe how Fadavi-Ardekani in combination with G.992.2 discloses determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, and I incorporate my analysis and opinions by reference. G.992.2 describes the relationship between the memory required by an interleaver and a corresponding deinterleaver, as I describe above with respect to the previous limitation. *See* G.992.2, § 7.6. This disclosure, combined with the disclosure of Fadavi-Ardekani, discloses to one of ordinary skill in the art how to determine, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

d. 5[d]. "allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate"

498. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:10-15; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

499. Above at Section IX.D.2.e, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data

rate. In addition, at Section IX.D.2.g above, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a second number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate. I incorporate both of those discussions by reference, and on that basis, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

e. **5[e]. "wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"**

500. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[e]. *See, e.g.*, G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. Above at Section IX.D.2.f, I explain how Fadavi-Ardekani in combination with G.992.2 discloses wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message, and I incorporate that discussion by reference. In the same way that the CO transceiver of Fadavi-Ardekani and G.992.2 would not allocate more memory for the interleaver than is specified in the messages that it exchanges during initialization, the transceiver would also not allocate more memory for the deinterleaver than is specified in the messages that it exchanges during initialization, in my opinion.

f. **5[f]. "allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes transmitted at a second data rate"**

501. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[f]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

502. Above at Section IX.D.2.g, I explain how Fadavi-Ardekani in combination with G.992.2 allocates a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes transmitted at a second data rate. Also,

at Section IX.D.2.e above, I explain how Fadavi-Ardekani in combination with G.992.2 discloses allocating a first number of bytes of the shared memory to an interleaver to interleave a first plurality of RS coded data bytes transmitted at a first data rate. I incorporate both of those sections herein by reference, and, on that basis, it is my opinion that the combination of Fadavi-Ardekani and G.992.2 discloses this limitation.

g. <u>5[g]. "deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the shared memory allocated to the interleaver"</u>

503. Fadavi-Ardekani in combination with G.992.2, in my opinion, discloses limitation 5[g]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

504. Above at Section IX.D.2.h, I explain how Fadavi-Ardekani in combination with G.992.2 discloses interleaving a first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, and I incorporate that discussion by reference. Though this limitation recites a first plurality being deinterleaved, and a second plurality of data bytes being interleaved, in my opinion, there is no difference in how a transceiver would implement this limitation. Therefore, it is my opinion that Fadavi-Ardekani and G.992.2 disclose this limitation.

h. <u>5[h]. "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver"</u>

505. Fadavi-Ardekani in combination with G.992.2 discloses limitation 5[h]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-7:33; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1.

506. I explain above at Section IX.D.2.i how it is my opinion that Fadavi-Ardekani in view of G.992.2 discloses "wherein the shared memory allocated to the interleaver is used at the

same time as the shared memory allocated to the deinterleaver," and I incorporate that discussion by reference herein. In my opinion, one of ordinary skill in the art would have understood that there is no difference between these two limitations, i.e., they both require that the deinterleaver and interleaver memory be used at the same time. Accordingly, it is my opinion that this limitation is met by Fadavi-Ardekani in combination with G.992.2.

4. <u>Claim 13 of the '882 Patent</u>

507. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 13 of the '882 patent, as I explain below.

a. <u>13[a]. "A system that allocates shared memory"</u>

508. To the extent that this preamble is limiting, Fadavi-Ardekani in combination with G.992.2 discloses a system that allocates shared memory. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3.

509. This preamble is identical to the preamble of claim 1 of the '048 patent, and for the same reasons, it is my opinion that the preamble is disclosed by Fadavi-Ardekani in view of G.992.2. *See* Section IX.D.2.a.

b. <u>13[b]. "a transceiver that performs"</u>

510. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses a transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67. This limitation is identical to the second limitation of claim 1 of the '048 patent, except that it recites "a transceiver that performs" additional steps. In my opinion, this limitation is met for the same reasons that I explain above at Section IX.D.2.b, and I incorporate my opinions herein by reference.

c. <u>13[c] through 13[i].</u>

511. These limitations are identical to the corresponding limitations of claim 5 of the '381 patent that I discuss above at Sections IX.D.3.c through IX.D.3.i (claim 1) and Sections

IX.B.4.b through IX.B.4.h (claim 5), and I incorporate those opinions herein by reference. *See* Appx. 3 (comparing limitations of claim 5 of the '381 patent with limitations of claim 13 of the '882 patent). For the same reasons, it is my opinion that these limitations are met by Fadavi-Ardekani in combination with G.992.2.

5. <u>Claim 19 of the '473 Patent</u>

512. In my opinion, Fadavi-Ardekani in combination with G.992.2 discloses each limitation of claim 19 of the '473 patent.

a. <u>19[a]. "An apparatus comprising"</u>

513. To the extent that the preamble is limiting, Fadavi-Ardekani discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, Fadavi-Ardekani at Abstract; col. 1:12-14; col. 2:18-24; col. 2:62-67. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.a.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

514. It is my opinion that Fadavi-Ardekani discloses a multicarrier communications transceiver. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:62-67; G.992.2, §§ 4.1, 4.2, 5, Fig. 2. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.b.

515. G.992.2 similarly discloses a transceiver, an ADSL transceiver unit (ATU) that complies with the G.992.2 standard. *See* G.992.2, §§ 4.1, 4.2, Fig. 2. G.992.2 explains that "[t]he ATU shall transport a single duplex bearer channel," which would indicate to one of ordinary skill in the art that the ATU is capable of transmitting and receiving data. ADSL systems, such as G.992.2, would be recognized by one of ordinary skill in the art as being multicarrier communications systems. One of ordinary skill in the art would further have

understood that the transmitter and receiver portions share some common circuitry, such as, for example, an interface to the subscriber line.

c. 19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

516. Fadavi-Ardekani in combination with G.992.2 discloses limitation 19[c], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 6:66-7:33. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.c.

517. Similarly G.992.2 discloses a duplex connection that includes both an upstream path and a downstream path. *See* G.992.2, § 5 ("The ATU shall transport a single duplex bearer channel. The bearer channel data rate shall be programmable in multiples of 32 kbit/s."). The upstream path and the downstream path are associated with an interleaver and a deinterleaver. *See id.* at § 7.6, § 7.3.1 ("The framing is equivalent to the 'reduced overhead mode with merged fast and sync bytes' as defined in Recommendation 7.4.4.2/G.992.1 using only the 'interleave buffer' definition."); § 7.3.3 ("A cyclic redundancy check (crc), scrambling, forward error correction (FEC) coding and interleaving shall be applied to the contents of the superframe."). One of ordinary skill in the art would have understood that these upstream and downstream paths are associated with interleaving and deinterleaving functions.

518. Therefore, Fadavi-Ardekani in combination with G.992.2 discloses this limitation, in my opinion.

d. 19[d]. "the multicarrier communications transceiver being associated with a memory"

519. In my opinion, Fadavi-Ardekani discloses limitation 19[d]. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3. I incorporate by reference my

analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.d.

e. 19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

520. Fadavi-Ardekani, in combination with G.992.2, discloses limitation 19[e], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.e.

521. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then the combination of Fadavi-Ardekani and G.992.2 discloses this limitation under TQ Delta's interpretation of the claims.

522. One of ordinary skill in the art would have understood that ADSL transceivers described in G.992.2 were capable of sending messages, including initialization messages, specifying communications parameters in ADSL systems. For example, G.992.2 teaches transceivers that exchange initialization messages that contain information about the channel as well as the transceivers and their capabilities and requirements. G.992.2, § 11.1.1 ("In subsequent parts of the initialization, in order to maximize the throughput and reliability of this link, ADSL transceivers shall determine certain relevant attributes of the connecting channel and establish transmission and processing characteristics suitable to that channel. During

initialization each receiver can determine the relevant attributes of the channel through the transceiver training and channel analysis procedures."). This includes communicating to a far-end transceiver "the number of bits and relative power levels to be used on each DMT subcarrier, as well as any messages and final data rates information." *Id.*

523. G.992.2 describes exchanging messages between the transceivers in an iterative process to establish transmission parameters such as data rates and formats for the ATU-R. The C-RATES1 message defined in G.992.2 is a signal sent from the ATU-C, whose purpose "is to transmit four options for data rates and formats to the ATU-R." *Id.* at § 11.9.2. Each of the four options contains three fields, one of which is the RRSI field that "contains Reed-Solomon FEC and interleaver parameters." The RRSI contains ten entries, including the number of DFs per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleaver depth in codewords. *See id.*; *see also* Table 26, Table 27.

524. An additional initialization message is the C-RATES-RA message, which sends "four new options for transport configuration for both upstream and downstream. These options will, in general, be closer to the optimum bit rate for the channel than those in C-RATES1. . . ." G.992.2, § 11.11.3. Like the C-RATES1 message, the C-RATES-RA message contains ten entries, including the numbers of data frames (DFs) per Reed-Solomon codeword in the downstream direction, downstream interleave depth in codewords, the number of DFs per Reed-Solomon codeword in the upstream direction, and the upstream interleave depth in codewords. *See id.*; *see also* Table 33, Table 34. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory

is allocated to the deinterleaving function." As with the parameters in the C-RATES1 message, one of ordinary skill in the art would have understood that the information in the C-RATES-RA message can be used to allocate memory between an interleaver and a deinterleaver function, at least within TQ Delta's interpretation of the claims.

f. **19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."**

525. Fadavi-Ardekani, in combination with G.992.2, discloses limitation 19[f], in my opinion. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 8:58-9:3; G.992.2, §§ 7.6, 11.1.1, 11.9.2, 11.11.3. I incorporate by reference my analysis and opinion regarding how Fadavi-Ardekani meets this element above at Section IX.C.6.f.

526. Additionally, one of ordinary skill would have understood that G.992.2 discloses that the interleaver memory and the deinterleaver memory are used at the same time. G.992.2 establishes a "single duplex bearer channel." G.992.2, § 5. One of ordinary skill in the art would have understood that data is transmitted in both directions at the same time. As a result, the interleaver and deinterleaver are both used at the same time, which in turn, means that the interleaver memory and deinterleaver memory are used at the same time. Accordingly, it is my opinion that Fadavi-Ardekani in combination with G.992.2 discloses this limitation.

6. **Motivation to Combine Fadavi-Ardekani and G.992.2**

527. One of ordinary skill in the art would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 in the manner claimed. First, both references are in the telecommunications field, and relate to ADSL systems specifically. *See, e.g.*, Fadavi-Ardekani, Abstract, col. 2:63-3:4; col. 4:9-21; col. 4-25:63 (describing an ADSL communication system); col. 4:65-5:40 (describing head-end ADSL transceiver); G.992.2, §§ 1

("The requirements of the Recommendation apply only to a single asymmetric digital subscriber line (ADSL)."); 4.1 ("The system reference model shown in Figure 1 describes the functional blocks required to provide ADSL service."); FIG. 1, FIG. 2. In addition, Fadavi-Ardekani references G.992.2 a number of times, confirming that one of ordinary skill in the art would naturally consider the references together. *See, e.g.*, Fadavi-Ardekani, col. 6:19-23 ("All functionalities of the FCI are provided as per ADSL standards. In a preferred embodiment of the invention, approximately four G.lite (ITU G.992.2) or approximately four ADSL (ANSI T1.413-1998) sessions are supported by the FCI."); col. 1:51-60 ("Many DSL technologies require that a signal splitter be installed at a remote end user location to split POTS service from the digital data transmission. However, the line split for an end user can be managed remotely from a central office using G.Lite (a/k/a DSL Lite, splitterless ADSL, and Universal ADSL), which is essentially a slower form of ADSL. Equipment installation costs are saved using G.Lite (ITU-T standard G-992.2), which provides a data rate of approximately 1.5 Mbps downstream and approximately 512 Kbps upstream."); col. 4:59-63 ("An exemplary digital communication system employing G.lite is similar to FIG. 1, with splitters 130, 134 and 146 merely replaced by a hardware device providing a direct correction to ADSL transceivers 128, 136, and 148 respectively."); col. 7:6-13 ("A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions."). For this reason, one of ordinary skill in the art would naturally have looked to G.992.2 when considering Fadavi-Ardekani.

528. Second, both references describe the need to allocate memory between interleaving and deinterleaving functions. *See, e.g.*, Fadavi-Ardekani, col. 5:57-6:6; col. 6:55-65; col. 7:25-30; col. 8:58-9:3, G.992.2, §§ 7.6; 11.1.1. Thus, both Fadavi-Ardekani and G.992.2 relate to the problem to be solved identified by the Family 3 patents – allocating shared memory between interleaving and deinterleaving functions. *See, e.g.*, '048 patent, col. 1:48-59 ("One difficulty with implementing multiple latency paths in a transceiver is the fact that a latency path is a complicated digital circuit that requires a large amount of memory and processing power. An interleaver within a latency path can consume a large amount of memory in order to provide error correcting capability."). One of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating and allocating memory between interleaver and deinterleaver functions when considering G.992.2 and its description of using interleavers and exchanging parameters, such as interleaver parameters, relating to transceivers during initialization.

529. Third, one of ordinary skill in the art, when considering Fadavi-Ardekani, would have naturally looked to G.992.2, and specifically to determine how to allocate shared memory. Fadavi-Ardekani discloses reducing the difficulty of the interleaving/deinterleaving process as a goal. *See, e.g.*, Fadavi-Ardekani, col. 3:1-4 ("Utilizing this buffering and scheduling methodology, reductions in the design sizes of various transceiver components and the data flow complexity of the transceiver may be achieved."). Fadavi-Ardekani faults prior art systems for being "excessively duplicative in terms of transceivers and memory in each transceiver, and thus more costly than necessary to provide the desired functionality." *Id.* at col. 2:57-59. It also discloses that reducing the amount of memory needed is desirable. *Id.* at col. 3:43-47; col. 8:4-12; 9:20-23. To do so, Fadavi-Ardekani discloses sharing one memory for

both interleaving and deinterleaving. *See, e.g., id.* at Abstract; col. 3:39-41; col. 7:25-30; col. 9:18-20.

530. Fadavi-Ardekani further explains that the amount of memory required by, and the allocation of memory between, the interleaver and deinterleaver depends on the services to be supported. Fadavi-Ardekani, col. 6:66-7:33 ("In a preferred embodiment of the invention, the IDIM is allocated as 10 K×16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G.lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention."). One of ordinary skill would have recognized that, in order to allocate memory between interleaver and deinterleaver functions in a useful way, the transceiver would need information about the amount of memory needed for the services that were to be supported by the transceiver.

531. As I describe above, G.992.2 discloses that the transceivers share information about the relevant attributes of the channel between them and the parameters they will use for interleaving and deinterleaving. *See, e.g.*, G.992.2, §§ 7.6, 11.1.1, 11.9.2 (describing C-RATES1 message); 11.11.3 (describing C-RATES-RA message). One of ordinary skill in the art would have been motivated to look to the teachings of G.992.2 for ways of exchanging interleaver parameters, such that memory can be shared as described in Fadavi-Ardekani.

E. <u>Claim 19 of the '473 Patent Is Obvious Over Voith in Combination with LB-031</u>

532. It is my opinion that claim 19 of the '473 patent is obvious over U.S. Patent No. 5,751,741 ("Voith") in combination with LB-031. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's

interpretation of the claims, however, then Voith in combination with LB-031 renders obvious claim 19 of the '473 patent.

1. **Brief Description of Voith**

533. Voith describes an ADSL transceiver that transmits and receives data using discrete multi-tone (DMT) multicarrier communications. *See*, *e.g.*, Voith at Abstract; col. 1:25-50; col. 2:61-64. A transmit section of the transceiver performs rate adaptation using a single rate adaptation buffer, without the need for multiple frame buffering. *Id.* at col. 2:64-67.

534. FIG. 2 of Voith, copied below, illustrates an ADSL transceiver with a digital interface unit, and FIG. 3 of Voith, also copied below, illustrates the digital interface unit.

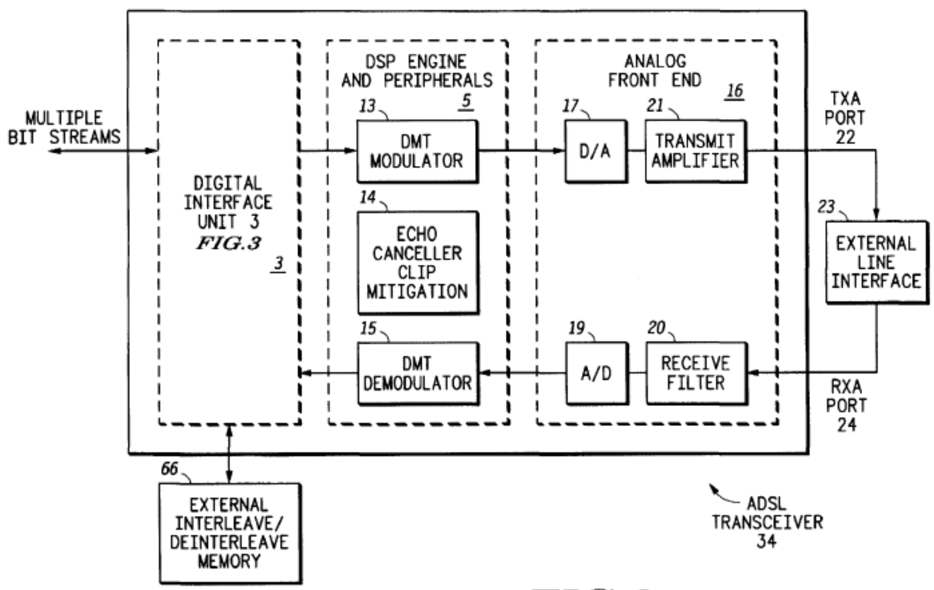


FIG.2

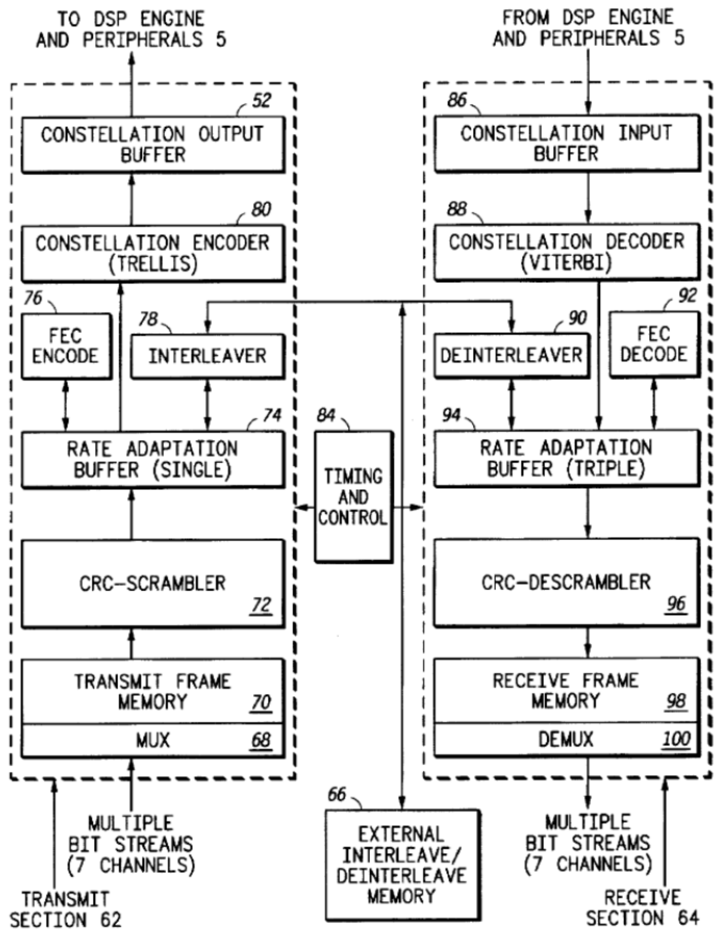


FIG.3

The digital interface unit has a transmit section and a receive section, which respectively "interleave[] transmit data and de-interleave[] receive data." *Id.* at col. 4:30-32; col. 4:44-45. Voith teaches that in order to accomplish the interleaving and deinterleaving, "ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66." *Id.* at col. 4:32-36.

535. The transceiver includes a common timing and control portion that coordinates the operation between the transmit and receive sections. *Id.* at col. 4:41-49; FIG. 3. A timing control block generates timing signals and also coordinates the activities of several modules in the transmit and receive paths so that their activities do not conflict. *Id.* at col. 4:50-55. The

timing control block also includes a memory arbitrator that arbitrates between the transmit and receive path for access to external interleave/deinterleave memory, "which is used by both transmit section 62 and receive section 64." *Id.* at col. 4:47-50; col. 4:55-58.

536. The transmit section of Voith's ADSL transceiver includes, among other things, an FEC encode block and an interleaver. *Id.* at col. 4:59-5:6; FIG. 3. The interleaver also has a bidirectional terminal connection to the external interleave/deinterleave memory. *Id.* at col. 5:6-8.

537. The receive section of Voith's ADSL transceiver includes, among other things, a deinterleaver and an FEC decode block. *Id.* at col. 5:13-17; FIG. 3. Like the interleaver, the deinterleaver has a bidirectional terminal connection to the external interleave/deinterleave memory. *Id.* at col. 5:21-23.

538. The FEC encoder of Voith "performs a forward error correction encoding first on fast data and next on interleaved data in the frame and appends redundancy bytes to the frame and stores those in appropriate portions of the rate adaptation buffer." *Id.* at col. 5:58-62. The interleaver operates only on the interleave portion of the frame, and both reads data out of and writes data back into the rate adaptation buffer. *Id.* at col. 5:62-65. Because the interleaving operation requires a large amount of memory, the interleaver uses a portion of the external interleave/deinterleave memory, and arbitrates with the deinterleaver so that only one external memory interface using common integrated circuit pins is required. *Id.* at 5:65-6:4. Voith's memory thus is allocated between the interleaving function and the deinterleaving function, in which at least a portion of the memory may be allocated to the interleaving function or deinterleaving function at any one particular time.

539. In the receive section of Voith's transceiver, a deinterleaver performs a deinterleave operation on the interleaved portion of the received frame. *Id.* at col. 6:24-26. The deinterleaver "makes use of external interleave/deinterleave memory" and "arbitrates for usage thereof in a manner similar to" the interleaver. *Id.* at col. 6:26-29. The FEC decode "first performs an FEC decode operation on the fast portion of the frame data, and then performs an FEC decode operation on the interleaved portion of the frame data." *Id.* at col. 6:29-32. If the FEC decode detects an error in the frame data, it performs correction within the rate adaptation buffer. *Id.* at col. 6:32-34.

2. <u>Claim 19 of the '473 Patent</u>

540. In my opinion, Voith in combination with LB-031discloses each limitation of claim 19 of the '473 patent.

a. <u>19[a]. "An apparatus comprising"</u>

541. In my opinion, to the extent that the preamble is limiting, Voith in combination with LB-031 discloses an apparatus, a multicarrier communications transceiver, as described below. *See, e.g.*, Voith at Abstract; col. 1:25-50; col. 2:61-67; FIGS. 2-3.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

542. It is my opinion that Voith in combination with LB-031 discloses limitation 19[b]. *See, e.g.*, Voith, Abstract; col. 1:25-30; col. 2:61-3:9; Figs. 2, 3; LB-031, p. 3, 4.

543. One of ordinary skill in the art would have understood that Voith discloses a multicarrier communications transceiver because it discloses an ADSL transceiver that implements DMT, which is a type of multicarrier modulation. *See, e.g.*, Voith, Abstract (noting that transceiver can receive data at 4.05 kHz); col. 1:25-37 ("Discrete multi-tone (DMT) is a multi-carrier technique which divides the available bandwidth of twisted-pair copper media connections into mini-subchannels or bins. . . ."); col. 2:61-3-9; FIGS. 2-3.

544. I explained above in Section IX.A.6.b why, in my opinion, LB-031 discloses a multicarrier communications transceiver, namely a VTU-O and a VTU-R. *See* LB-031 at pp. 3, 4. I incorporate by reference my analysis and opinion from that section.

545. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

c. 19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"

546. In my opinion, Voith in view of LB-031, discloses limitation 19[c]. *See, e.g.*, Voith, col. 4:42-48; col. 4:59-5:12; col. 5:58-6:4; LB-031, pp. 2, 3.

547. Voith describes the signal processing in the transmit section as being "defined by the ADSL standard" and describes the framing of separate fast and interleaved data into DMT symbols for transmission. *See, e.g.*, Voith at col. 5:40-6:4 ("[S]even channels of payload data are then stored in corresponding portions of transmit frame memory 70. In addition, transmit frame memory 70 appends a FAST byte and a SYNC byte, defined by the ADSL standard, at the appropriate points in the frame. . . . CRC-scrambler 72 performs an 8-bit cyclic redundancy check first on the fast data and then on the interleaved data. The scrambler function of CRC-scrambler 72 also operates first on the fast data and next on the interleaved data. . . . FEC encode 76 performs a forward error correction encoding first on fast data and next on the interleaved data in the frame and appends redundancy bytes to the frame and stores those in appropriate portions of rate adaptation buffer 74. Interleaver 78 operates only on the interleave portion of the frame, and reads data out of rate adaptation buffer 74 and writes data back into rate adaptation buffer 74 after performing the interleaving operation. Because the interleaving operation requires a large amount of memory, interleaver 78 uses a portion of external interleave/deinterleave memory 66. Interleaver 78 arbitrates for use of external

interleave/deinterleave memory 66 with deinterleaver 90 so that only one external memory interface using common integrated circuit pins is required."). I understand that the Court has construed the term "latency path" to mean "transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay." As a skilled artisan would have understood as of the Family 3 patents' priority date, the fast data and interleaved data are each associated with a separate latency path, each with a distinct latency. Therefore, the transmit section of Voith handles two latency paths, one of which is interleaved.

548. The receive section of Voith processes the received data similarly and also handles two latency paths, fast and interleaved. *See, e.g.*, *id.* at col. 6:24-34 (in receive section, "[a] deinterleaver 90 performs a deinterleave operation on the interleaved portion of the received frame. Deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78. FEC decode 92 first performs an FEC decode operation on the fast portion of the frame data, and then performs an FEC decode operation on the interleaved portion of the frame data. If FEC decode 92 detects an error in the frame data, it performs correction within rate adaptation buffer 94."). Thus, the receive section of Voith also handles two latency paths, one of which is interleaved, each of which has a distinct latency. Consequently, Voith discloses a multicarrier communications transceiver that is configured to perform an interleaving function associated with a first latency path (the interleaved path in the transmit direction) and perform a deinterleaving function associated with a second latency path (the interleaved path in the receive direction).

549. As I explained above in Section IX.A.6.c, LB-031 also teaches a transceiver that is configured to perform an interleaving function associated with a first latency path, and a

deinterleaving function associated with a second latency path. *See*, *e.g.*, LB-031 at pp 2, 3. I incorporate by reference my analysis and opinion from that section.

550. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

d. 19[d]. "the multicarrier communications transceiver being associated with a memory"

551. In my opinion, Voith alone or in view of LB-031 discloses limitation 19[d]. *See, e.g.*, Voith, col. 4:21-40; col. 4:59-5:39; Fig. 3; LB-031, pp. 3, 4.

552. FIG. 3 of Voith illustrates a memory associated with the transceiver, an "external interleave/deinterleave memory 66, which is used by both transmit section 62 and receive section 64." Voith, col. 4:49-50. Voith specifically notes that the "[i]nterleaver 78 also has a second bidirectional terminal connected to external interleave/deinterleave memory 66," and that the "[d]e-interleaver 90 has a first bidirectional terminal, and a second bidirectional terminal connected to external interleave/deinterleave memory 66." Voith, col. 5:5-7; 5:21-23; *see also id.* at col. 4:21-40; FIG. 3.

553. I explained above in Section IX.A.6.d why, in my opinion, LB-031 also teaches the multicarrier communications transceiver being associated with a memory. *See*, *e.g.*, LB-031 at pp. 3, 4. I incorporate by reference my analysis and opinion from that section.

554. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

e. 19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

555. Voith, in combination with LB-031, discloses limitation 19[e], in my opinion. *See, e.g.*, Voith, col. 5:58-6:43; LB-031, at p. 3.

556. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Voith in combination with LB-031 discloses this limitation under TQ Delta's interpretation of the claims.

557. Voith discloses allocating memory between the interleaving function and the dinterleaving function. *See, e.g.*, Voith, at col. 5:58-6:43. Voith specifically notes that "[b]ecause the interleaving operation requires a large amount of memory," the interleaver "uses a portion of external interleave/deinterleave memory 66." *Id.* at col. 5:65-6:1. Voith also discloses that its interleaver "arbitrates" with the deinterleaver for use of external the interleave/deinterleave memory. *Id.* at col. 6:1-4. Voith also discloses that a deinterleaver performs a deinterleave operation on the interleaved portion of the received frame. *Id.* at col. 6:24-26. Voith's deinterleaver "makes use of external interleave/deinterleave memory 66" and "arbitrates for usage thereof" in a manner similar to the interleaver. *Id.* at col. 26-29. It is my understanding that the Court construed the term "memory is allocated between the interleaving function and the deinterleaving function" to mean "an amount of memory is allocated to the interleaving function and an amount of memory is allocated to the deinterleaving function."

558. LB-031 teaches the well-known principle that the amount of memory required to meet a particular interleaver delay requirement depends on the line data rate. *See* LB-031 at p. 4. The line data rate, in turn, depends on the number of bits assigned to each subcarrier. Voith discloses that "[t]he bit allocation table is determined at initialization between the central office

and the remote terminal based on the characteristics of the transmission link." Voith, col. 6:9-12. As a person having ordinary skill in the art would have understood as of the Family 3 patents' priority date, the bit allocation table is determined during initialization by the receiving transceiver and communicated to the transmitting transceiver in a message sent during the initialization procedure. Therefore, Voith discloses that the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver, at least within TQ Delta's interpretation of the claims in its infringement contentions.

559. I explained above in Section IX.A.6.e why, in my opinion, LB-031 also discloses allocating a memory between the interleaving function and the deinterleaving function. *See*, *e.g.*, LB-031 at p. 3. I incorporate by reference my analysis and opinion from that section.

560. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

f. 19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

561. Voith, in view of LB-031, discloses limitation 19[f], in my opinion. *See, e.g.*, Voith, col. 4:50-58; col. 5:58-6:43; LB-031, p. 3.

562. Voith specifically explains that a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. Voith, col. 5:65-6:4 ("Because the interleaving operation requires a large amount of memory, interleaver 78 uses a portion of external interleave/deinterleave memory 66. Interleaver 78 arbitrates for use of external interleave/deinterleave memory 66 with deinterleaver 90 so that only one external memory interface using common integrated circuit pins is required."); *id.* at col. 4:50-58

("Timing control block 84 generates timing signals which are necessary for the signal processing functions. Timing control block 84 also coordinates the activities of several modules in both the transmit and receive path so that their activities do not conflict. Furthermore, timing control block 84 includes a memory arbitrator that arbitrates between the transmit and receive path for access to external interleave/deinterleave memory 66."); *id.* at col. 6:26-29 ("Deinterleaver 90 makes use of external interleave/deinterleave memory 66 and artibrates for usage thereof in a manner similar to interleaver 78."); *id.* at col. 4:35-41 ("in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations."); *id.* at col. 4:30-32 ("As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive data.").

563. As noted above, Voith also discloses that memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver. *Id.* at col. 5:58-6:43. Consequently, at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

564. I explained above in Section 244 why, in my opinion, LB-031 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. *See*, *e.g.*, LB-031 at p. 3. I incorporate by reference my analysis and opinion from that section.

565. Accordingly, it is my opinion that the combination of Voith and LB-031 discloses this limitation.

3. <u>Motivation to Combine Voith and LB-031</u>

566. In my opinion, one of ordinary skill in the art would have been motivated to combine Voith and LB-031 for at least the following reasons. First, each is in the telecommunications field. Each discloses sharing memory for interleaving and deinterleaving to support various applications. *See, e.g.*, Voith, col. 4:29-58; col. 5:65-6:4; *see also* LB-031 at p. 2 ("The smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver [3]. Typically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same."); *id.* at p. 3 ("The size of the interleaver memory will be a major source of complexity in VDSL2."); *id.* at p. 4 ("Suppose a VDSL2 transceiver supports up to 44.5 Mbit/s as a line data rate. If the minimum interleaver delay requirement were 5.23ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of at least 14546 octets according to equation (2) (although this is actually implementation specific).").

567. Thus, in my opinion, both Voith and LB-031 relate to the problem purportedly addressed by the '473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, '473 patent at col. 1:37-45; *id.* at col. 1:48-60. One of ordinary skill in the art would naturally have considered these complementary references together.

568. Furthermore, LB-031 explains that "[t]he interleaver is a major source of complexity in VDSL2," (LB-031 at p. 1), and Voith discloses that efficiency in the use and management of memory is desirable. *See, e.g.*, Voith, at col. 2:26-28 ("[L]arge buffers consume a large integrated circuit area which adds to its cost."); *see also id.* at col. 4:30-40 ("As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive data. In order to perform these complex functions, ADSL transceiver 34 requires a large

amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66. Also, in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations.”). LB-031, meanwhile, discloses the desirability of balancing efficiency and performance. *See, e.g.,* LB-031 at p. 3 (“Equations (2), (4), (5), and (6) illustrate trade-offs between interleaver memory, error correction capability, delay, and burst separation. More interleaver memory normally allows more error correction but leads to higher delays and a longer separation between error bursts. Significant error correction can be achieved by using shorter codewords requiring less memory, less delay, and shorter time between bursts. However, small codewords typically have lower net coding gain and higher computation requirements since there are more decoder operations required in the same amount of time. Therefore, we make a trade-off between complexity, capability, and performance.”).

569. In my opinion, one of ordinary skill in the art would have naturally considered the advantages of each of these references, including their common goals of allocating memory for interleaving and deinterleaving operations, and would have been motivated to combine them. One of ordinary skill in the art considering Voith would have naturally looked to LB-031 to determine an effective and efficient way to allocate memory between interleaving and deinterleaving functions, including allocating memory at any one particular time depending on the message. One of ordinary skill in the art would have had a reasonable expectation that this combination would work and would be relatively straightforward to implement. There would have been substantial motivation to combine these references prior to the invention date.

F. Claim 19 of the '473 Patent is Obvious In View of Mazzoni and G.993.1.

570. It is my opinion that Mazzoni in combination with G.993.1 discloses each limitation of claim 19 of the '473 patent. I explain below at Section IX.F.4 why it is my opinion that one of ordinary skill in the art would have been motivated to combine Mazzoni and G.993.1. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Mazzoni in combination with G.993.1 renders obvious claim 19 of the '473 patent.

1. Brief Description of Mazzoni

571. I provided a brief description of Mazzoni above in Section IX.B.2, which I incorporate by reference.

2. Brief Description of G.993.1

572. I provided a brief description of G.993.1 above in Section VII.F.4, which I incorporate by reference.

3. Claim 19 of the '473 Patent

573. In my opinion, Mazzoni in combination with G.993.1discloses each limitation of claim 19 of the '473 patent.

a. 19[a]. "An apparatus comprising"

574. In my opinion, and to the extent that this preamble is limiting, Mazzoni in combination with G.993.1 discloses an apparatus, a multicarrier communications transceiver, as I describe below.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

575. It is my opinion that Mazzoni in combination with G.993.1 discloses a multicarrier communications transceiver. *See, e.g.*, Mazzoni, col. 1:8-27; G.993.1 §§ 4; 5.2, 6.7, 8.5.1, 9.2.1, Fig. 5-2.

576. As I explain above in Section IX.B.6.b, which I hereby incorporate by reference here, Mazzoni discloses that its invention "may advantageously applied to a very high rate digital subscriber line (VDSL) environment or system," which a person having ordinary skill in the art would have understood to include VDSL transceivers according to G.993.1. *See* Mazzoni, col. 1:19-21. Similarly, I have also explained how G.993.1 discloses a VDSL transceiver, which employs multicarrier communications, at Section IX.C.6.b, which I also incorporate by reference here.

577. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

c. <u>19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"</u>

578. It is my opinion that Mazzoni in combination with G.993.1 discloses limitation 19[c]. *See, e.g.*, Mazzoni, col. 3:62-4:25; Fig. 3; G.993.1, §§ 8.4.1, 8.4.2.

579. I explain above at Section IX.B.6.c, which I hereby incorporate by reference here, how it is my opinion that Mazzoni discloses an interleaving function associated with a first latency path, and a deinterleaving function associated with a second latency path, by explaining that its VDSL communication system allows the operator to provide multiple symmetrical and asymmetrical services. In addition, I explain above that G.993.1 discloses transceivers that are configured to support multiple latency paths and perform interleaving and deinterleaving

functions using a convolutional interleaver associated with those latency paths (see Section IX.C.6.c). I incorporate my previous discussion and opinions by reference.

580. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

d. <u>19[d]. "the multicarrier communications transceiver being associated with a memory"</u>

581. Mazzoni in combination with G.993.1 discloses limitation 19[d], in my opinion. *See, e.g.*, Mazzoni, col. 1:59-2:24; col. 2:37-48; col. 2:57-3:4; col. 5:9-20; Fig. 3, 4, 5; G.993.1, § 8.4.1.

582. It is my opinion, as I explain above at Section IX.B.6.d, which I hereby incorporate by reference, that this limitation is met by Mazzoni's memory associated with an interleaving and deinterleaving means, which may be a RAM such as a dual-port memory. *See, e.g.*, Mazzoni, col. 2:57-60. In addition, G.993.1 discloses memory associated with an interleaver and deinterleaver pair, as I describe in Section IX.C.6.d, which I also incorporate by reference.

583. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

e. <u>19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"</u>

584. In my opinion, Mazzoni in combination with G.993.1 discloses limitation 19[e]. *See, e.g.*, Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

585. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message

described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Mazzoni in combination with G.993.1 discloses this limitation under TQ Delta's interpretation of the claims.

586. I previously explained that Mazzoni discloses how the memory allocation can be determined, and reconfigured, based on the bit rate processed by a modem, above at Section IX.B.6.e, which I incorporate by reference. *See* Mazzoni, col. 1:61-65; col. 5:24-31. G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver, as I explain above at Section IX.C.6.e, which I also incorporate by reference.

587. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

f. <u>19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"</u>

588. It is my opinion that Mazzoni and G.993.1 disclose limitation 19[f]. *See, e.g.*, Mazzoni, col. 1:59-65; col. 2:3-18; col. 5:21-30; G.993.1, §§ 8.4.1, 8.4.2.

589. Above, I explain how Mazzoni discloses allocating distinct portions of a common memory to an interleaver and a deinterleaver, such that a portion is used by either function at any particular time, according to the message, at Section 339, which I incorporate by reference. G.993.1 similarly teaches that a portion of memory can be allocated to an interleaver and a deinterleaver, which I explain above at Section IX.C.6.f, and incorporate by reference.

590. Accordingly, it is my opinion that the combination of Mazzoni and G.993.1 discloses this limitation.

4. **Motivation to Combine Mazzoni and G.993.1**

591. In my opinion, one of ordinary skill in the art would have been motivated to combine Mazzoni and G.993.1, as I explain below.

592. First, Mazzoni and G.993.1 are both specifically directed to VDSL and to VDSL transceivers. G.993.1 was the first of the ITU-T's specifications for VDSL transceivers, and the title of Mazzoni is "Device for Sending/Receiving Digital Data Capable of Processing Different Bit Rates, in Particular in a VDSL Environment."

593. Second, each of Mazzoni and G.993.1 discloses a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Mazzoni, col. 1:8-15 ("Moreover, the invention relates to sending and receiving digital data that can have different bit rates, and to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates."); col. 1:54-65 ("Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates."); G.993.1 at § 5.1, p. 5 ("The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies."); §

8.4.1, p. 15 ("The same size interleaving memory… is needed for interleaving at the transmitter and de-interleaving at the receiver.").

594. Thus, both references relate to the problem purportedly addressed by the '473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, '473 Patent at col. 1:37-45; col. 1:48-60. As a result, one of ordinary skill in the art would naturally have considered Mazzoni and G.993.1 together.

595. Mazzoni describes how sharing memory between interleaving and deinterleaving functions is advantageous, and that optimizing the size of the memory is advantageous. *See, e.g.*, Mazzoni, col. 1:54-65 ("Still another object of the invention is to provide such an architecture which is adaptable, particularly in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates. These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)."). Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers. One of ordinary skill in the art would have recognized that conveying interleaver parameters through the initialization message scheme of G.993.1 would avoid this limitation of Mazzoni's table and would result in a more flexible solution.

G. Claim 19 of the '473 Patent is Obvious In View of Voith and G.993.1, or, In the Alternative, In View of Voith, G.993.1 and Mazzoni.

596. It is my opinion that Voith in combination with G.993.1 discloses each limitation of claim 19 of the '473 Patent. In the alternative, and to the extent that the combination of Voith and G.993.1 is not deemed to disclose each limitation of claim 19 of the '473 patent, it is my opinion that Mazzoni supplies the missing teachings, as I explain below at Section IX.G.4. I explain below why one of ordinary skill in the art would be motivated to combine Voith with G.993.1, and Voith and G.993.1 with Mazzoni, below at Sections IX.G.3 and IX.G.5, respectively.

597. I have reviewed TQ Delta's infringement contentions for Family 3, and I do not agree with the interpretation of the claims that TQ Delta uses in its contentions. If the Court or other trier of fact does agree with TQ Delta's interpretation of the claims, however, then Voith in combination with G.993.1, or Voith in combination with G.993.1 and Mazzoni, renders obvious claim 19 of the '473 patent.

1. Brief Descriptions of Voith, G.993.1, and Mazzoni.

598. I provide a brief description of Voith above at Section IX.E.1, G.993.1 at Section VII.F.4, and Mazzoni at Section IX.B.2. I incorporate each of those sections herein by reference.

2. Claim 19 of the '473 Patent

a. 19[a]. "An apparatus comprising"

599. In my opinion, and to the extent that this preamble is limiting, Voith in combination with G.993.1 discloses an apparatus, a multicarrier communications transceiver, as I describe below.

b. <u>19[b]. "a multicarrier communications transceiver"</u>

600. It is my opinion that Voith in combination with G.993.1 discloses a multicarrier communications transceiver. *See, e.g.*, Voith, col. 2:61-3:9; col. 1:44-50; G.993.1 §§ 4; 5.2, 6.7, 8.5.1, 9.2.1, Fig. 5-2.

601. As I explain above in Section IX.E.2.b, which I incorporate by reference, Voith discloses an ADSL multicarrier communications transceiver that employs DMT. Similarly, I have also explained how G.993.1 discloses a VDSL transceiver, which also specifies DMT, at Section IX.C.6.b, which I also incorporate by reference.

602. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

c. <u>19[c]. "that is configured to perform an interleaving function associated with a first latency path and perform a deinterleaving function associated with a second latency path"</u>

603. It is my opinion that Voith in combination with G.993.1 discloses limitation 19[c]. *See, e.g.*, Voith, col. 4:29-58; Fig. 3; G.993.1, §§ 8.4.1, 8.4.2.

604. I explain above at Section IX.E.2.c, which I incorporate by reference, how it is my opinion that Voith discloses an interleaving function associated with a first latency path, and a deinterleaving function associated with a second latency path. In addition, I explain above how G.993.1 discloses how transceivers are configured to support multiple latency paths, and perform interleaving and deinterleaving functions using a convolutional interleaver, associated with those latency patents at Section IX.C.6.c, which I also incorporate by reference.

605. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

d. 19[d]. "the multicarrier communications transceiver being associated with a memory"

606. Voith in combination with G.993.1 discloses limitation 19[d], in my opinion. *See, e.g.*, Voith, col. 3:55-65; col. 4:29-58; Fig. 2, 3; G.993.1, § 8.4.1.

607. It is my opinion, as I explain above at Section IX.E.2.d, which I incorporate by reference, that this limitation is met by Voith's external interleave/deinterleave memory. In addition, G.993.1 discloses memory associated with an interleaver and deinterleaver pair, as I describe in Section IX.C.6.d, which I also incorporate by reference.

608. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

e. 19[e]. "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

609. In my opinion, Voith in combination with G.993.1 discloses limitation 19[e]. *See, e.g.*, Voith, col. 5:65-6:4; G.993.1, §§ 8.4.1, 8.4.2, 12.4.1, 12.4.6.1, 12.4.6.2.1.1, 12.4.6.3.1.1.

610. I have reviewed TQ Delta's infringement contentions for this claim, and I understand TQ Delta asserts that this limitation is met by receiving the O-PMS message described in VDSL2. I do not agree that receiving the O-PMS message meets this limitation, and I do not agree with TQ Delta's infringement read. If the Court or other trier of fact interprets the claim such that the O-PMS message meets this limitation, however, then Voith in combination with G.993.1 discloses this limitation under TQ Delta's interpretation of the claims.

611. I explain how Voith discloses allocating the external interleave/deinterleaver memory, while using an arbitration procedure between the two functions to do so, above at

Section IX.E.2.e, which I incorporate by reference. G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver, as I explain above at Section IX.C.6.e, which I also incorporate by reference.

612. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

f. **19[f]. "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"**

613. It is my opinion that Voith and G.993.1 disclose limitation 19[f]. *See, e.g.*, Voith, col. 5:64-6:4; G.993.1, §§ 8.4.1, 8.4.2.

614. Above, I explain how Voith discloses allocating its memory to an interleaver and a deinterleaver, such that a portion is used by either function at any particular time depending on the message at Section IX.E.2.f, which I incorporate by reference. G.993.1 similarly teaches that a portion of memory can be allocated to an interleaver or a deinterleaver depending on the message, which I explain above at Section IX.C.6.f, which I also incorporate by reference.

615. Accordingly, it is my opinion that the combination of Voith and G.993.1 discloses this limitation.

3. **Motivation to Combine Voith and G.993.1**

616. In my opinion, one of ordinary skill in the art would have been motivated to combine Voith and G.993.1, as I explain below.

617. First, each of the references is in the DSL field, and each discloses a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Voith, col. 4:29-41 ("As part of the ADSL task, digital interface unit 3 also interleaves transmit data and de-interleaves receive

data. In order to perform these complex functions, ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66. Also, in order to minimize the number of integrated circuit pins required to access external memory, the interleave and de-interleave buffers are also preferably implemented in the same physical memory and digital interface unit 3 preferably multiplexes between interleaving and de-interleaving operations. . . ."); col. 4:51-58; col. 5:65-6:4; G.993.1 at § 5.1, p. 5 ("The reference configuration provides two or four data paths with bit rate under the control of the network operator, consisting of one or two downstream and one or two upstream data paths. A single path in each direction can be of high latency (with lower BER expected) or lower latency (with higher BER expected). Dual paths in each direction provide one path of each type. The dual latency configuration is thought to be the minimum that is capable of supporting a sufficient full service set, although there are organizations supporting both the single latency model with programmable latency, and others requesting more than two paths/latencies."); § 8.4.1, p. 15 ("The same size interleaving memory… is needed for interleaving at the transmitter and de-interleaving at the receiver.").

618. Thus, both references relate to the problem purportedly addressed by the '473 patent—allocating memory for interleaving and deinterleaving to support various applications. *See, e.g.*, '473 Patent at col. 1:37-45; col. 1:48-60. As a result, one of ordinary skill in the art would naturally have considered these references together. Further, Voith discloses that efficiency in the use of memory is desirable. *See, e.g.*, Voith at col. 1:44-47; col. 2:26-35.

619. As discussed above, G.993.1 discloses how memory is allocated in accordance with a message received during initialization. One of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the

transceivers of Voith to partition the shared memory between the interleaver and deinterleaver. By exchanging information about their available memory, using messaging like that disclosed in G.993.1, the transceivers of Voith would be able to determine an appropriate allocation of the available memory to the interleaver and deinterleaver.

620. One of ordinary skill in the art would have had a reasonable expectation that this combination would work and would be relatively straightforward to implement. For example, adding G.993.1 messaging scheme to a transceiver according to Voith would be relatively simple, as one of ordinary skill in the art would have understood, particularly in view of Voith's reference to ADSL, which also uses messaging during initialization to enable the ATU-C and ATU-R to exchange information regarding their interleaving and deinterleaving requirements and capabilities.

4. <u>Mazzoni Supplies Any Disclosure Missing from G.993.1 and Voith</u>

621. To the extent that any limitations of claim 19 of the '473 patent are not disclosed by G.993.1 and Voith, it is my opinion that they are supplied by Mazzoni.

622. With respect to limitation 19[e], Mazzoni provides additional description on how memory is allocated between an interleaving function and a deinterleaving function. For example, Mazzoni discloses that the interleaver/deinterleaver memory has a memory allocation that "can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)." Mazzoni, col. 1:61-65. Furthermore, Mazzoni discloses that "the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means" are determined "according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′)." *Id.* at col. 5:24-31. When combined with the disclosure of Voith and G.993.1, this discloses a

means of allocating the memory between the interleaving function and the deinterleaving function.

623. With respect to limitation 19[f], Mazzoni discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message. Mazzoni discloses a memory that can be shared between the interleaving and deinterleaving means. Mazzoni, col. 1:59-65 ("These and other objects, features, and advantages are provided by a memory means whose size is optimized for a global (send+receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem)."); col. 2:57-50 ("The memory may be a random access memory, such as a dual-port memory, for example. The interleaving means and the deinterleaving means may respective include first addressing means and second addressing means."). One of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time and that a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

5. <u>Motivation to Combine Mazzoni with Voith and G.993.1.</u>

624. I explain above at Section IX.G.3, which I incorporate by reference, that one of ordinary skill in the art would have been motivated to combine Voith and G.993.1. Additionally, one of ordinary skill in the art would have been motivated to combine the teachings of Mazzoni with both of Voith and G.993.1.

625. Like Voith and G.993.1, Mazzoni is in the DSL field, and it describes a need to allocate memory for interleaving and deinterleaving. *See, e.g.*, Mazzoni, col. 1:8-15; col. 1:54-65. Mazzoni, like Voith and G.993.1, thus addresses the problem purportedly addressed by the

’473 patent – the allocation of memory for interleaving and deinterleaving to support different applications. *See, e.g.*, ’473 patent, col. 1:37-45; col. 1:48-60.

626. Further, Voith discloses that efficiency in the use of memory is desirable. *See, e.g.*, Voith at col. 1:44-47; col. 2:26-35. Mazzoni, meanwhile, discloses that an adaptable architecture is advantageous, and that optimizing the size of memory is advantageous. *See, e.g.*, Mazzoni at 1:54-65. Mazzoni futher discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the tranceiver. *See, e.g.*, Mazzoni at col. 6:51-61. One of ordinary skill would have recognized the inherent limitations of Mazzoni’s table, namely that all services would need to be identified ahead of time so that the table could be created and stored in the transceiver.

627. As discussed above, G.993.1 discloses how memory is allocated in accordance with a message received during initialization. One of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni. Instead, by exchanging information about their available memory, using messaging like that disclosed in G.993.1, the transceivers of Mazzoni would determine an appropriate allocation of the available memory to the interleaver and deinterleaver.

628. Thus, is it my opinion that one of ordinary skill in the time of the invention would have been motivated to combine the teachings of Mazzoni with the teachings of Voith and G.993.1.

X. <u>SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS</u>

629. I understand that TQ Delta and its experts may present evidence relating to secondary considerations of non-obviousness, for example, while contending that the references

described above in my report do not render obvious the asserted claims of the Family 3 patents. I have reviewed TQ Delta's Supplemental Responses to Defendants' Joint Interrogatory Nos. 4, 8, and 12, which inquire about secondary considerations of non-obviousness.

630. If TQ Delta should present evidence regarding secondary considerations of non-obviousness in support of the non-obviousness of the Family 3 patents, whether in its responsive expert reports, or at a later date, I reserve the right to address this evidence in my reply report, or any supplemental reports thereafter.

XI. CONCLUSION

631. In my opinion, based on my review of the Family 3 patents, the materials referenced herein, and my knowledge of what a person of ordinary skill in the art would have known at and before each of the Family 3 patents' priority dates about the technology at issue, a person of ordinary skill in the art would have understood all of the claim elements and limitations of claim 1 of the '048 patent, claim 5 of the '381 patent, claim 13 of the '882 patent, and claim 19 of the '473 patent to be obvious over (a) LB-031; (b) LB-031 in combination with Mazzoni; (c) Fadavi-Ardekani in combination with G.993.1; and (d) Fadavi-Ardekani in combination with G.992.2. It is also my opinion that a person of ordinary skill in the art would have understood all of the claim elements and limitations of claim 19 of the '473 patent to be obvious over (a) Voith in combination with LB-031; (b) Mazzoni in combination with G.993.1; and (c) Voith in combination with G.993.1, or in the alternative, Voith in combination with G.993.1 and Mazzoni. I further opine that the asserted claims are invalid for indefiniteness, lack of enablement, and lack of written description as I explain above.

632. I reserve the right to supplement my opinions in the future to respond to any arguments or positions that TQ Delta or its experts may raise, taking account of new information as it becomes available to me.

Executed in Campbell, CA.

Date: November 28, 2018

Krista S. Jacobsen

APPENDIX A

Krista S. Jacobsen

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Experience

JACOBSEN IP LAW, Campbell, CA (February 2014 - present)
Attorney and Counselor at Law. Solo practitioner providing expert consultant, expert witness, patent litigation support, patent prosecution, and intellectual property (IP) counseling services.

SANTA CLARA UNIVERSITY SCHOOL OF LAW, Santa Clara, CA (January 2015 - present)
Lecturer in Law. Co-teaching Pretrial Litigation Techniques (Fall 2015, Fall 2016, Fall 2017, Fall 2018) and Law Practice Management (Spring 2015, Spring 2016, Spring 2017, Spring 2018).

DISRUPTIVE FORCE LLC, Campbell, CA (February 2015 - present)
Co-founder and CEO.

HEADWATER PARTNERS, Redwood Shores, CA (July 2011 - February 2014)
Head Counsel. Responsibilities included general counsel duties and patent prosecution.

COVINGTON & BURLING, LLP, Redwood Shores, CA (October 2009 - July 2011)
Associate. IP litigation.

HELLER EHRMAN, Menlo Park, CA (May-July 2008)
Summer Associate. IP litigation. Researched and drafted legal memoranda and briefs.

BLAKELY SOKOLOFF TAYLOR & ZAFMAN, Sunnyvale, CA (June-August 2007)
Summer Associate. Patent prosecution. Composed responses to United States Patent and Trademark Office office actions and wrote portions of patent applications, including claims.

CONSULTANT (July 2004 - September 2007)
Responsibilities included assisting clients to determine and execute digital subscriber line (DSL) standardization and product strategies, writing simulations, generating and presenting technical tutorials, drafting and prosecuting patent applications, and helping with other patent issues. Clients included 2Wire, Inc., PMC-Sierra, Atheros Communications, and Beyer Law Group.

TEXAS INSTRUMENTS (TI) (formerly AMATI COMMUNICATIONS), San Jose, CA (January 1994 - May 2004).

Lead xDSL Standards Strategist (2001-04)

- Led TI's DSL standardization efforts, managed standards resources and budget, and communicated standards progress and status within TI.
- Developed and presented dozens of technical proposals for regional and international standards organizations, including ETSI TM6, ITU-T SG15/Q4, T1E1.4, and IEEE 802.3ah (Ethernet in the first mile).
- Wrote DSL white papers, technical reports, technical book chapters, and articles for external publications.
- Participated as a member of business unit patent committee and worked with TI legal department to ensure protection of intellectual property and to provide technical assistance.
- Wrote and ran DSL system simulations.
- Made presentations at industry conferences and events.

Previous roles with Amati/TI were *Project Manager, ADSL over ISDN* (2000-01), *Project Manager, VDSL* (1999-2000), *Senior Staff Engineer* (1998-99), *Staff Engineer* (1997-98), *Senior Systems Engineer* (1996-97), *Consultant* (1994-96).

VITEL COMMUNICATIONS CORPORATION, Santa Clara, CA (August 1991 - May 1992).
Member of telecommunications group. Worked on a team that developed a video telephony transceiver.

Bar Memberships and Registrations

STATE BAR OF CALIFORNIA
Member No. 267868 (admitted December 7, 2009)

COLORADO STATE BAR
Registration No. 43,294 (admitted May 24, 2011 (currently inactive))

UNITED STATES PATENT AND TRADEMARK OFFICE
Registration No. 59,374 (registered October 11, 2006)

Krista S. Jacobsen

Education

SANTA CLARA UNIVERSITY SCHOOL OF LAW (Santa Clara, CA)

JD (*magna cum laude*), 2009

Honors and Awards

Santa Clara University School of Law Intellectual Property (IP) Fellowship (2006-09)
Dean's List (2006-09)
Order of the Coif (2009)
ABA-BNA Award for Excellence In the Study of Intellectual Property Law (Spring 2008)
CALI Award for Excellence In: Managing Complex IP Litigation (Fall 2008), IP Litigation Techniques (Spring 2008), Patent Prosecution (Spring 2008), Protection of IP (Spring 2008), Advocacy (Fall 2007), Contracts (Spring 2007)
Witkin Award for Excellence In: Opening Statements and Closing Arguments (Fall 2008), Pretrial Litigation Techniques (Fall 2008), Mass Communication (Fall 2007), Property (Spring 2007), Legal Analysis, Research and Writing, Section H (Spring 2007)
Grand Prize, First Annual San Francisco Intellectual Property Law Association Student Writing Competition (February 2009)
Selected to represent Santa Clara University in the Dean Jerome Prince Memorial Evidence Moot Court Competition (Spring 2009) and Constance Baker Motley National Moot Court Competition in Constitutional Law (Spring 2008)

Activities

Co-President, Santa Clara University Student Intellectual Property Law Association (2008-09)
Vice President, Alumni Relations, Santa Clara University Intellectual Property Association (2007-08)
Associate, Santa Clara Computer and High Tech Law Journal (2007-08)

STANFORD UNIVERSITY (Stanford, CA)

Ph.D. in electrical engineering, 1996

Dissertation: *Discrete Multi-Tone-Based Communications in the Reverse Channel of Hybrid Fiber-Coax Networks*
Adviser: John M. Cioffi (http://www.stanford.edu/group/cioffi)

MSEE, 1993

Digital communications specialization

Honors and Awards

IBM Graduate Fellowship (1994-95)
National Science Foundation Graduate Fellowship (1991-94)
IEEE Communications Society Scholarship (1993)

UNIVERSITY OF DENVER (Denver, CO)

BSEE (*summa cum laude*), 1991

Communications specialization

Honors and Awards

Winner, Denver Section IEEE Student Paper Contest (1991)
University of Denver Pioneer Award (1991)
University of Denver Distinguished Senior Woman Award (1990)
Phi Beta Kappa (1988)
University of Denver Honors Scholarship (1986-91)
Colorado Scholars Scholarship (1987-91)

Publications

LAW REVIEW AND JOURNAL PAPERS

Krista S. Jacobsen, *Intellectual Property in Standards: Does Antitrust Law Impose a Duty to Disclose (Even If the Standards-Setting Organization Does Not)?*, 26 Santa Clara Computer & High Tech. L.J. 459 (2010).

Krista S. Jacobsen, *Methods, Marking, and Messiness: Revisiting the Federal Circuit's Rule That Product Marking is not Required Where a Patent is Directed to a Method*, 13 U.S.F. Intell. Prop. L. Bull. 107 (2009).

Krista S. Jacobsen

TECHNICAL BOOKS

Implementation and Applications of DSL Technology (Philip Golden, Herve Dedieu, and Krista S. Jacobsen, eds., Auerbach Publications, 2008): Co-author of chapter 17, entitled “DSL Standardization,” and author of the ADSL portion of that chapter.

Fundamentals of DSL Technology (Philip Golden, Herve Dedieu, and Krista S. Jacobsen, eds., Auerbach Publications, 2006): Author of chapter 7, entitled “Fundamentals of Multi-carrier Modulation.”

Broadband Last Mile Access Technologies for Multimedia Communications (Nikil Jayant, ed., CRC Press, 2005): Author of chapter 3, entitled “Last Mile Copper Access.”

Cable Modems: Current Technologies and Applicatons (John Fijoleck, Michelle Kuska, Venkata C. Majeti, and Kotikalapudi Sriram, eds., IEEE Press, 1999): Co-author of Part II, section 3, entitled “Synchronized Discrete Multitone Modulation for Upstream Transmission on Cable Networks.”

Author of the definition of “broadband communication” in *World Book Encyclopedia* (2003).

TECHNICAL JOURNAL PAPERS AND MAGAZINE ARTICLES

K.S. Jacobsen. “Patents and Standardization, Part 3: Commitments to License Standard-Essential Patents Under Reasonable and Non-Discriminatory (RAND) Terms.” *IEEE Communications Magazine - Communications Standards Supplement*, September 2016, pp. 66-71.

K.S. Jacobsen. “Patents and Standardization, Part 2: Duties to Disclose Patents to Standards Development Organizations.” *IEEE Communications Magazine - Communications Standards Supplement*, July 2016, pp. 18-23.

K.S. Jacobsen. “Patents and Standardization, Part 1: A Tutorial on Patents.” *IEEE Communications Magazine - Communications Standards Supplement*, March 2016, pp. 10-14.

B. Wiese and K.S. Jacobsen. “Use of the Reference Noise Method Bounds the Performance Loss Due to Upstream Power Backoff.” *IEEE Journal on Selected Areas in Communications*, vol. 20, no. 5, June 2002, pp. 1075-84.

N.P. Sands and K.S. Jacobsen. “Pilotless Timing Recovery for Baseband Multi-carrier Modulation.” In *IEEE Journal on Selected Areas in Communications*, vol. 20, no 5., June 2002, pp. 1047-54.

K.S. Jacobsen. “Methods of Upstream Power Backoff on Very High-Speed Digital Subscriber Lines.” In *IEEE Communications Magazine*, vol. 39, no. 3, March 2001, pp. 210-16.

J.M. Cioffi *et al.* “Very-high-speed Digital Subscriber Lines.” In *IEEE Communications Magazine*, vol. 37, no. 4, April 1999, pp. 72-79.

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K.S. Jacobsen. “Design and Performance of Synchronized DMT (SDMT) Modems for VDSL.” In *ICCE Conference Record*, Los Angeles, CA, June 1999.

K.S. Jacobsen. “Synchronized DMT (SDMT) for Very high-speed Digital Subscriber Line (VDSL) Transmission.” In *Globecom ’98 Conference Record*, Sydney, Australia, November 1998.

K.S. Jacobsen. “Discrete Multi-Tone Modulation for High-Speed Upstream Communications on HFC Networks.” In *Conference Record of the Thirty-First Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 1997.

K.S. Jacobsen. “Synchronized Discrete Multi-Tone (SDMT) Modulation for Cable Modems: Making the Most of the Scarce Reverse Channel Bandwidth.” In *Wescon ’97 Conference Proceedings*, Santa Clara, CA, November 1997.

K.S. Jacobsen and J.M. Cioffi. “Achievable Throughput of Multicarrier-based Multipoint-to-point Networks Using a Reservation-based Channel Access Protocol.” In *Globecom ’96 Conference Record*, London, U.K., November 1996.

K.S. Jacobsen, J.A.C. Bingham and J.M.Cioffi. “Synchronized DMT for Multipoint-to-point Communications on HFC Networks.” In *Globecom ’95 Conference Record*, Singapore, November 1995.

Krista S. Jacobsen

J.A.C. Bingham and K.S. Jacobsen. “Upstream Transmission in an HFC System using SDMT: the Network, Data Rates, and a MAC Protocol.” Presented at Globecom ’95, Singapore, November 1995.

K.S. Jacobsen *et al.* “Very High Bit Rate Digital Subscriber Lines (VDSL): An Effective Deployment Strategy for FTTC Utilizing the Existing Copper Network.” In *Proceedings of VII International Workshop on Optical Access Networks*, Nuremberg, Germany, September 1995.

K.S. Jacobsen, J.A.C. Bingham and J.M. Cioffi. “A Discrete Multitone-based Network Protocol for Multipoint-to-point Digital Communications in the CATV Reverse Channel.” In *Canadian Cable Television Association (CCTA) Cablexpo Technical Papers*, Halifax, Nova Scotia, May 1995.

K.S. Jacobsen and J.M. Cioffi. “An Efficient Digital Modulation Scheme for Multimedia Transmission on the Cable Television Network.” In *Technical Papers, 43rd Annual National Cable Television Association (NCTA) Convention and Exposition*, New Orleans, LA, May 1994.

K.S. Jacobsen and J.M. Cioffi. “High-performance Multimedia Transmission on the Cable Television Network.” In *Proceedings 1994 International Conference on Communications*, New Orleans, LA, May 1994.

Patents

A.J. Redfern, G. Ginis, F.A. Mujica, and K.S. Jacobsen. “Spectrally flexible band plans with reduced filtering requirements.” U.S. Patent Number 7,342,937. March 2008.

K.S. Jacobsen, M.D. Agah, and B.R. Wiese. “Method to mitigate effects of ISDN off/on transitions in ADSL.” U.S. patent number 7,184,467. February 2007.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. “Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system.” U.S. patent number 7,110,370. September 2006.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. “Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system.” U.S. patent number 7,079,549. July 2006.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. “Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system.” U.S. patent number 7,068,678. June 2006.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. “Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system.” U.S. patent number 6,937,623. August 2005.

K.S. Jacobsen, B. Wiese, and C. Milbrandt. “Upstream power back-off.” U.S. patent number 6,922,448. July 2005.

J.M. Cioffi, J.A.C. Bingham, and K.S. Jacobsen. “Method and apparatus for coordinating multi-point to-point communications in a multi-tone data transmission system.” U.S. patent number 6,473,438. October 2002.

B. Wiese, K.S. Jacobsen, N.P. Sands, and J. Chow. “Initializing communications in systems using multi-carrier modulation.” U.S. patent number 6,434,119. August 2002.

K.S. Jacobsen and B. Wiese. “A method to mitigate the near-far FEXT problem.” U.S. patent number 6,205,220. March 2001.

J.A.C. Bingham and K.S. Jacobsen. “Methods for coordinating upstream discrete multi-tone data transmissions.” U.S. patent number 5,644,573. July 1997.

Prior Testimony

***TC Technology LLC v. Sprint Corp. and Sprint Spectrum, L.P.* (D. Del., Case No.: 16-cv-00153-RGA)**
Provided fact witness deposition testimony.

***TQ Delta, LLC v. 2Wire, Inc.* (D. Del., Case No.: 13-cv-1835-RGA)**
Provided testimony at Markman hearing on behalf of defendant 2Wire.

***In re Marriage of Prince* (Sup. Ct. Cal., County of Santa Clara, Case No.: 2012-1-FL-163041)**
Provided deposition and trial testimony on behalf of Petitioner, Jeffrey Prince.

APPENDIX B

008 FH (12783725)
041 FH (11860080)
048 FH
09710310 (627 parent app) FH
12255713 (008 parent app) FH
12769193 (835) FH
13914852 (162) FH
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337 FH (13156098)
379 FH (11232899)
379 provisional (60613594)

381 FH
412 FH (12779660)
427 FH (13439605)
430 FH (12477742)
473 FH
511 FH (12783777)
610 FH (13284549)
627 FH (11211535)
686 FH (10619691)
706 FH (12769277)
721 FH (11863581)
778 FH (12783771)
784 FH (12779708)
784 provisional (60174865)
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804 provisional
881 FH (10264258)
881 provisional (60327440)
882 FH
890 FH
890 provisional (60618269)
956 FH (13476310)
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B. Ray, R. Abbi, Definitions of Managed Objects for High Bit-Rate DSL - 2nd generation (HDSL2) and Single-Pair High Speed
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Cisco Systems, Inc. v. TQ Delta, LLC, Petition for Inter Partes Review, IPR2016-01007, filed May 6, 2016
Claim Construction Order for Family 1 Patents, dated February 6, 2018
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D. Divsalar & J. H. Yuen, Performance of Concatenated Reed-Solomon/Viterbi Channel Coding, TDA Progress Report 42-71
D. Rauschmayer, "Adsl/Vdsl Principles: A Practical and Precise Study of Asymmetric Digital Subscriber Lines and Very High
David Krinsky Deposition Transcript and Exhibits 501 through 510, dated November 29, 2017
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Defendant 2Wire, Inc.'s Invalidity Contentions in Response to TQ Delta's July 2, 2018 Final Infringement Contentions and
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Defendant 2Wire, Inc.'s Opening Brief in Support of its Motion for Judgment on the Pleadings, dated December 22, 2016
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EP 1 792 430
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G.992.2
G.992.3 (1999)
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G.996.1 (2001)
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Kevin Russell Deposition Transcript and Exhibits 600 through 638
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Mark Roche Deposition Transcript and Exhibits 1 through 23, dated September 12, 2018
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Michael Lund Deposition Transcript and Exhibits 518 through 527, dated November 30, 2017
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Order re: the Court's contemplated Family 2 Claim Constructions, dated October 30, 2017
Parties' Joint Claim Construction Brief for Family 2 Patents, dated August 30, 2017
Parties' Joint Claim Construction Brief for the Family 1 Patents, dated August 22, 2017
Parties' Joint Claim Construction Brief for the Family 3 Patents, dated September 6, 2017
Parties' Joint Supplemental Claim Construction Brief for the Family 1 Patents, dated December 20, 2017
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Plaintiff TQ Delta, LLC's Supplemental Claim Charts 1-17, 20, 23, 26-31, 33-42, and 45-51, and new chart 52, dated May 22,
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Plaintiff's Family 1 Claim Construction Demonstratives, dated September 5, 2017
Plaintiff's Family 2 Claim Construction Demonstratives, dated November 2, 2017

Plaintiffs' Notice of Supplemental Authority for Family 2 Claim Construction, dated October 31, 2017
Plaintiffs' Notice of Supplemental Authority for Family 3 Claim Construction, dated November 10, 2017
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S. Haykin, Communication Systems, 3rd Ed. (1994)
Scott Voegele Deposition Errata Corrections, dated May 2, 2018
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U.S. Patent No. 7,831,890
U.S. Patent No. 7,835,430
U.S. Patent No. 7,836,381
U.S. Patent No. 7,844,882
U.S. Patent No. 7,889,784
U.S. Patent No. 7,925,958

U.S. Patent No. 7,978,706
U.S. Patent No. 7,979,778
U.S. Patent No. 8,073,041
U.S. Patent No. 8,090,008
U.S. Patent No. 8,218,610
U.S. Patent No. 8,238,412
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U.S. Patent No. 8,355,427
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U.S. Patent No. 8,495,473
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U.S. Pub. No. 2003/0185212
U.S. Pub. No. 2006/0245366
US 6,658,052 File History (ultimate parent)
US20020006128A1
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US5251210
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US5608733
US6002670
US6115386
US6178448
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US6707822B1 (Fadavi-Ardekani)
US6731678B1
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US6772388B2
US6788686B1
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WO2006044227 (ISR+WO)

APPENDIX C

APPENDIX C – Comparison of Family 3 Patent Claim Language ('882, '381 and '048 Patents)

U.S. Patent No. 7,844,882 Claim 13	U.S. Patent No. 7,836,381 Claim 5	U.S. Patent No. 8,276,048 Claim 1
13[a]. A system that allocates shared memory comprising:	5[a]. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:	1[a]. A system that allocates shared memory comprising:
13[b]. a transceiver that performs:		1[b]. a transceiver that is capable of:
13[c]. transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;	5[b]. transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver;	1[c]. transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver;
13[d]. determining an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;	5[c]. determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory;	1[d]. determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory;

U.S. Patent No. 7,844,882 Claim 13	U.S. Patent No. 7,836,381 Claim 5	U.S. Patent No. 8,276,048 Claim 1
13[e]. allocating a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,	5[d]. allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for ~~transmission~~ [reception] at a first data rate,	1[e]. allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate,
13[f]. wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;	5[e]. wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;	1[f]. wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message;
13[g]. allocating a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and	5[f]. allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes ~~received~~ [transmitted] at a second data rate; and	1[g]. allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate; and
13[h]. deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the interleaver,	5[g]. deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and interleaving the second plurality of RS coded data bytes within the ~~shred~~ [shared] memory allocated to the interleaver,	1[h]. interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver,

U.S. Patent No. 7,844,882 Claim 13	U.S. Patent No. 7,836,381 Claim 5	U.S. Patent No. 8,276,048 Claim 1
13[i]. wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.	5[h]. wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.	1[i]. wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

EXHIBIT 10

FILED UNDER SEAL

EXHIBIT 10

FILED UNDER SEAL

UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

TQ Delta, LLC, Plaintiff, v. 2Wire, Inc. Defendant.	Case No. C.A. No. 1:13-cv-01835-RGA Jury Trial Demanded

REBUTTAL EXPERT REPORT OF DR. TODOR COOKLEV REGARDING VALIDITY OF THE FAMILY 3 PATENTS

CONFIDENTIAL – ATTORNEYS' EYES ONLY

I declare under penalty of perjury that the following is true and correct.

DECEMBER 28, 2018	
DATE	Todor Cooklev, Ph.D.

I. INTRODUCTION

1. My name is Dr. Todor Cooklev, and I have been retained by TQ Delta LLC ("TQ Delta").

2. I have been asked to prepare this report ("Rebuttal Report") in connection with the above captioned District Court action between TQ Delta LLC and 2Wire, Inc. ("Defendant"). I have reviewed the report by Dr. Krista Jacobsen ("the Jacobsen Report") submitted in this litigation on November 29, 2018. I address the Jacobsen Report in detail below. Specifically, I have been asked to opine on Dr. Jacobsen's allegations that the claim 1 of U.S. Patent No. 8,276,048 ("the '048 patent"), claim 5 of U.S. Patent No. 7,836,381 ("the '381 patent"), claim 13 of U.S. Patent No. 7,844,882 ("the '882 patent"), and claim 19 of U.S. Patent No. 8,495,473 ("the '473 patent") are invalid. I will be referring to the above-mentioned claims, collectively, as the Asserted Claims, and to the above-mentioned patents, collectively, as the Asserted Patents or the Family 3 Patents.

3. My qualifications were described in detail in Section II of my opening report on the infringement of the Family 3 Patents submitted on November 28, 2018 ("Cooklev Inf. Report"), as well as in my curriculum vitae, which was attached to that Report as Exhibit 1.

4. I also incorporate my discussion of the Asserted Claims and claim constructions from my opening report. *See, e.g.*, Cooklev Inf. Report at §§ VII.D-F, X.

5. In coming to my conclusions, I reviewed the materials identified in Exhibit 1 to this Report, as well as all materials referenced in this Report.

6. As detailed below, based upon my personal knowledge, expertise, and the review and analysis I have performed to date, I have formed the following opinions:

7. Claim 1 of the ’048 patent is valid. The claim cover patentable subject matter, is obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification’s written description, enabled, and definite.

8. Claim 5 of the ’381 patent is valid. The claim cover patentable subject matter, is obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification’s written description, enabled, and definite.

9. Claim 13 of the ’882 patent is valid. The claim cover patentable subject matter, is obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification’s written description, enabled, and definite.

10. Claim 19 of the ’473 patent is valid. The claim cover patentable subject matter, is obvious in view of the prior art as applied by Dr. Jacobson. The claim is supported by the specification’s written description, enabled, and definite.

11. I set forth below the bases and reasoning for these opinions. Specifically, I explain why Dr. Jacobson’s opinions fail to invalidate the Asserted Claims on any basis. In doing so, I explain why each alleged prior art reference does not invalidate the Asserted Claims, by obviousness, and why the Asserted Claims are not invalid for lack of written description or enablement, or for indefiniteness.

12. I based this Report on information currently available to me. I reserve the right to expand, modify, or supplement my Report based on additional information, to the extent that information was not provided to me before this Report is due. I further

reserve the right to expand, modify, and/or supplement this Report and my opinions in response to matters raised by Defendant and/or Defendant's expert(s), opinions provided by other defendants and/or their expert(s) in related matters, or in view of relevant orders and findings by the Court.

13. In this Report, I cite to various documents and testimony. These citations are meant to be exemplary, and not exhaustive. Citations to documents or testimony are not intended to signify that my conclusions or opinions are limited to the cited sources, or supported by the cited sources only.

14. I expect to be available for deposition and to testify at trial in the above captioned actions. I reserve the right to perform demonstrations and use animations, demonstratives, and/or other physical evidence at trial. I expressly reserve the right to offer opinions at trial and/or in one or more supplemental reports on subjects raised in my deposition, as well as on matters raised by Dr. Jacobsen or by Defendant(s) in any subsequent report, at deposition, or at trial.

15. I am being compensated at $420 per hour, which is my standard hourly consulting rate, plus reasonable expenses. I have not received any additional compensation for my work on this case, and no part of my compensation is dependent on my conclusions or on the outcome of the above captioned actions.

II. APPLICABLE LEGAL PRINCIPLES

16. I have reviewed Dr. Jacobsen's statements of legal standards that Dr. Jacobsen purportedly applied in forming her opinions. While I generally agree with the statements on the law, the summarizations overlook several important points that result

in misleading opinions. I have been informed by TQ Delta's counsel about the legal principles that I understand control the issues that Dr. Jacobsen opined on and which I rebut. I have applied these legal standards to the facts, circumstances, and materials considered, along with my experience, in reaching the conclusions and opinions expressed in this Report.

A. Presumption of Validity

17. It is my understanding that the claims of an issued U.S. patent are presumed valid. I further understand that the party challenging a patent claim's validity bears the burden of proving that claim invalid by clear and convincing evidence.

18. I understand that the standard for clear and convincing evidence is higher than the preponderance-of-evidence standard that is used to determine infringement. I am informed that the clear-and-convincing evidence standard requires an abiding conviction that the truth of a fact is highly probable.

19. I understand that this burden may be more difficult for a Defendant to meet if prior art was considered by the Examiner during the original prosecution of an Asserted Patent.

B. Anticipation

20. I understand the following principles apply for determining anticipation under 35 U.S.C. § 102. A patent claim is anticipated by prior art when each element of the claim is present within a single prior art reference. In addition, each element of the claim must be arranged in the prior art as it is in the claim. An element may be either

expressly disclosed or inherent in the prior art. A claim element is only inherent if it is necessarily present in the reference. I further understand that the possibility, even if probable, that an element may result from a certain set of circumstances – that is, an element ***might*** be present – is not sufficient to establish inherency.

21. I have been informed that, although anticipation cannot be established through a combination of references, additional references may be used to interpret the allegedly anticipating reference by, for example, indicating what the allegedly anticipating reference would have meant to one of ordinary skill in the art. For the claim to be anticipated, however, these other references must make clear that the missing descriptive matter in the patent claim is necessarily or implicitly present in the allegedly anticipating reference, and that it would be so recognized by one of ordinary skill in the art.

C. Obviousness

22. I understand the following principles apply for determining obviousness under 35 U.S.C. § 103. A claim may be invalid as obvious if the difference between the claimed subject matter and one or more prior art references are such that the subject matter as a whole would have been obvious at the time the invention was made to a person of ordinary skill in the art ("POSITA"). The following factors must be found and considered in determining obviousness: (1) the scope and content of the prior art; (2) the differences between the art and the claims at issue; (3) the level of ordinary skill in the art; and, (4) objective evidence of non-obviousness, which is also referred to as secondary considerations.

23. It is not enough that the prior art references can be combined; there must be a motivation to one of ordinary skill in the art to arrive at the claimed invention. But I also understand that motivation may not be gleaned from impermissible hindsight reasoning. That is, the reason to combine the prior art to arrive at the claimed invention cannot be based in whole or in part on the inventors' own disclosure.

24. I understand that assessing which prior art references to combine and how they may be combined to match the asserted claim may not be based on hindsight reconstruction. Hindsight reconstruction is using the patent itself as a road map for recreating the invention. In assessing obviousness, only what was known before the invention was made can be considered. I also understand that one important guard against such hindsight reconstruction is a determination whether a person of ordinary skill in the art would have been motivated, taught, or suggested to combine the relevant techniques of the prior art to duplicate the patent claims at the time of the patented invention.

25. I understand that obviousness cannot be predicated on the mere identification in the prior art of individual components of claimed limitations. It is not appropriate to pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather, there must be some teaching or suggestion in the references to support their use in the particular claimed combination.

26. I understand that it is the Defendant's burden to prove that a person of ordinary skill in the art would have been motivated to combine the prior art references. I understand that the motivation to combine must be supported by evidence and

articulated explanation. When considering obviousness, I understand that it is insufficient to simply say that a skilled artisan, once presented with a combination of references, would have understood that they could be combined.

27. Rather, the Defendant must show that the skilled artisan would have been motivated to make the combinations or modification of prior art to arrive at the claimed invention. Conclusory statements alone are insufficient, and any obviousness analysis must be supported by a reasoned explanation as to why a person of ordinary skill in the art would have been motivated to combine the prior art. For example, "common sense" or "intuition" alone cannot support a motivation to combine without explaining why they would lead a skilled artisan to solve the problem at hand with the particular elements of the claimed invention.

28. I understand that, to determine the scope and content of the prior art, I must consider whether the prior art was reasonably relevant to the particular problem the inventors faced in making the claimed invention.

29. To determine whether any material differences existed between the scope and content of the prior art and each asserted claim, I must consider the claimed invention as a whole to determine whether or not the claim would have been obvious in light of the prior art. If the prior art discloses all the elements in separate references, I must consider whether it would have been obvious to combine those references. I understand that a claim is not obvious just because all elements of a claim already existed.

30. I understand that a motivation to conduct further testing or research that may lead to the claimed invention does not necessarily render a claim obvious. I further understand that an invention is not necessarily rendered obvious simply because it was obvious to try a certain combination.

31. Secondary considerations may also impact a determination of obviousness, provided that there is some nexus or link between the claimed invention and the secondary factors considered. I further understand that any secondary factors that may prove instructive in determining non-obviousness should be considered. The following are examples:

(1) a long-felt, but unmet need for the invention;

(2) prior art teaching away from the invention;

(3) failure of others to make the invention;

(4) praise for the invention;

(5) commercial success;

(6) copying of the invention;

(7) initial skepticism for the invention;

(8) licensing;

(9) whether the invention proceeded in a direction contrary to accepted wisdom in the field.

32. I understand that the inquiry into secondary considerations is a means to check hindsight analysis. I am informed that it is impermissible to use hindsight and that it is improper to focus on just one portion or element of the invention, as opposed to the invention as a whole.

33. I also understand that when prior art teaches away from combining prior art references, the discovery of a successful way to combine them is unlikely to be obvious. Prior art teaches away from an invention when a person of ordinary skill would be discouraged or diverted from following the path leading to the invention because of the prior art. I also understand that if a proposed combination would require modification of prior art and that modification would render the prior art unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed combination and modification.

D. Written Description

34. I understand the following legal principles apply to assessing whether a patent is invalid for not meeting the written description requirement in 35 U.S.C. § 112, ¶ 1. The written description requirement evaluates whether the patent applicant had possession of the full scope of the claimed invention at the time the patent application was filed. This evaluation is made from the perspective of one of ordinary skill in the art. Claims may be broader than the embodiment or embodiments identified in the specification, and the specification may contain adequate written description of a broadly claimed invention without expressly describing every embodiment the claim encompasses.

E. Definiteness and Enablement

35. I also understand that claims must be particular and distinct, which is also referred to as a definiteness requirement in 35 U.S.C. § 112, ¶ 2. This definiteness requirement provides that a patent applicant must particularly point out and distinctly

claim the subject matter that the applicant regards as the invention. The definiteness standard is one of reasonableness under the circumstances. In other words, in light of the teachings of the prior art and of the particular invention, the definiteness inquiry is whether the claims inform those skilled in the art about the scope of the invention with reasonable certainty.

36. The enablement requirement requires the inventor to describe his or her invention in a manner that would allow others in the industry to make and use the invention. To analyze enablement, one needs to take into account the knowledge of a POSITA.

37. I understand that a patent need not teach, and preferably omits, what is well known in the art. I also understand that resort to material outside of the specification in order to satisfy the enablement requirement is permissible because it makes no sense to encumber the specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention. I further understand that the fact that some experimentation is necessary does not preclude enablement, but that any required experimentation must be reasonable. Some trial and error is permissible.

38. Further, I have been informed that enablement does not require the inventor to foresee every means of implementing an invention. Finally, I am informed that the specification need not necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can fill in any gaps, interpolate between embodiments, and even extrapolate beyond the disclosed embodiments.

F. Claiming Priority to A Provisional Application

39. I understand that a patent may be given the prior art date of the patent's provisional application. I am informed that a reference patent is entitled to claim the benefit of the filing date of its provisional application if the disclosure of the provisional application provides support for the claims in the reference patent.

III. PERSON OF ORDINARY SKILL IN THE ART

40. I defined a person of ordinary skill in the art with respect to the subject matter of the Family 3 Patents in Section VI.A of my Opening Infringement Report. I incorporate that definition by reference. *See* Cooklev Inf. Report at § VI.A.

IV. BACKGROUND OF DSL TECHNOLOGY AND INVENTION

41. I set forth a background of DSL communications, error correction, interleaver and deinterleaver memory, and the inventions of the Asserted Patents alongside with their befits in Sections VII.A-F of my Opening Infringement Report. *See* Cooklev Inf. Report at §§ VII.A-F. I incorporate those sections by reference.

A. Interleaver Memory and Deinterleaver Memory in Prior Art Systems

42. DSL systems, such as, for example, ADSL2/2+ standards known at the time of the inventions, specify dedicated interleaving memory requirements in each transceiver separately for upstream and downstream transmission (i.e. in each direction separately). More specifically, an ADSL2/2+ ATU-C is required to have a specified amount of dedicated interleaving memory for downstream data transmission and separately and independently have a specified amount of dedicated interleaving memory for upstream data reception. ADSL2/2+ specifies that the ATU-C must have

enough dedicated memory for downstream interleaving to interleave codewords sizes of Nfec= 255 bytes with an interleaver depth of D=64. This corresponds to Nfec x D=255 x 64 = 16,320 octets of dedicated interleaving memory for downstream. Likewise, ADSL2/2+ specifies that the ATU-C must separately have enough dedicated memory for upstream deinterleaving to deinterleave codewords sizes of Nfec= 255 bytes with an deinterleaver depth of D=8. This corresponds to Nfec x D=255 x 8 = 2,048 octets of dedicated deinterleaving memory for upstream. The total interleaving + deinterleaving memory requirement for an ATU-C is therefore approximately 16K + 2K = 20K. These requirements are specified (or derived from values provided) in Tables 7-7, 7-8, 7-9 and 7-10 of G.992.3/2002.

43. In the same manner, an ADSL2/2+ ATU-R is required to have a specific amount of dedicated interleaving memory for downstream data reception and separately have a specific amount of dedicated interleaving memory for upstream data transmission. Like the ATU-C, ADSL2/2+ specifies that the ATU-R must have enough dedicated memory for downstream deinterleaving to deinterleave codewords sizes of Nfec= 255 bytes with an deinterleaver depth of D=64. This corresponds to Nfec x D=255 x 64 = 16,320 octets of dedicated deinterleaving memory for downstream. Like the ATU-C, ADSL2/2+ specifies that the ATU-R must have enough memory for upstream interleaving to interleave codewords sizes of Nfec= 255 bytes with an interleaver depth of D=8 for upstream. This corresponds to Nfec x D=255 x 8 = 2,048 octets of dedicated interleaving memory. The total deinterleaving + interleaving memory requirement for

an ATU-R is therefore approximately 16,320 + 2,048 = 18,368 octets. These requirements are specified in Tables 7-7, 7-8, 7-9 and 7-10 of G.992.3/2002.

44. The ADSL2/2+ standards do not specify or enable memory sharing between the interleaver and the deinterleaver in a single transceiver. Furthermore, since ADSL2/2+ specify that the ATU-C downstream interleaver and the ATU-R downstream deinterleaver have the same amount of memory (i.e., ~16K octets) there are no messages specified (or ever needed) to negotiate the amount of memory to be allocated to the interleaver (in the ATU-C) or to the deinterleaver (in the ATU-R). Likewise, since ADSL2/2+ specify that the ATU-R upstream interleaver and the ATU-C upstream deinterleaver have the same amount of memory (i.e. ~2K octets) there are no messages specified (or ever needed) to negotiate the amount of memory to be allocated to the interleaver (in the ATU-R) or to the deinterleaver (in the ATU-C).

45. Prior to the inventions disclosed in the Family 3 patents, an amount of memory available to an interleaver was predetermined and an amount of memory available to a deinterleaver was predetermined. Those systems were incapable of sharing memory between an interleaving and deinterleaving function based on a message.

B. Shared Interleaver and Deinterleaver Memory in the Family 3 Patent Inventions

46. The below examples illustrate how, even if one of the transceivers provided more memory than the minimum specified by a standard, the interleaver memory and the deinterleaver memory in a single transceiver had been implemented in

prior art systems before the inventions of the Family 3 patents in comparison with how the shared memory can be allocated to an interleaver and a deinterleaver according to the inventions of the Family 3 patents.

47. Generally, a transceiver (e.g., VTU-R) with a larger dedicated deinterleaver memory than is required could at most determine whether a transceiver (e.g., VTU-0) at the other line of the line can also support a larger amount. But, if the VTU-O does not support a larger amount than is required, however, the extra deinterleaver memory of the VTU-R is simply not used. For example, it is not available to be used for the upstream interleaver function. The examples described below illustrate this concept.

48. Example 1 (Prior Art Systems). VTU-O (30,000 octets of dedicated downstream interleaver memory; 30,000 octets of dedicated upstream deinterleaver memory). VTU-R (40,000 octets of dedicated downstream deinterleaver memory; 20,000 octets of dedicated upstream interleaver memory).

Legend:

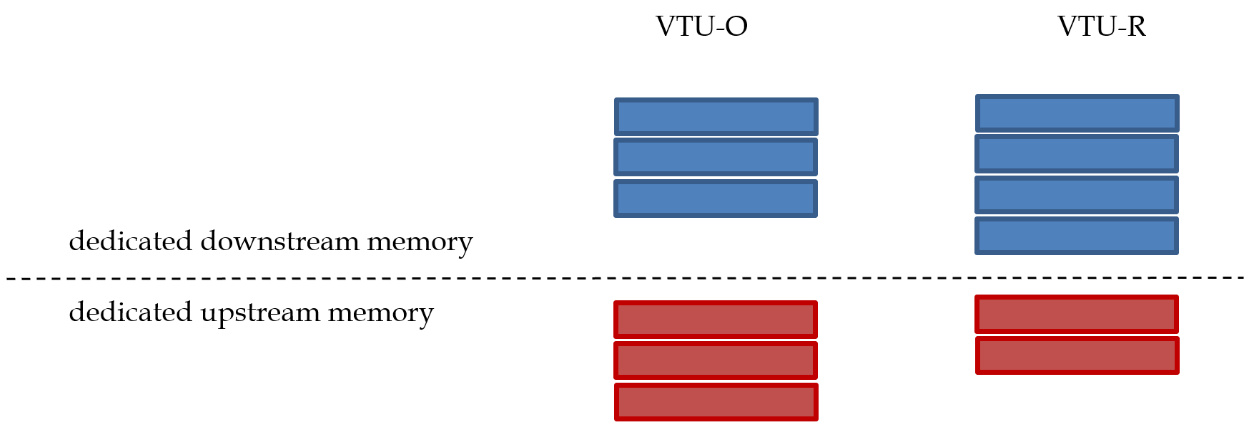
dedicated downstream memory (interleaver memory for VTU-O, deinterleaver memory for VTU-R)

dedicated upstream memory (interleaver memory for VTU-R, deinterleaver memory for VTU-O)

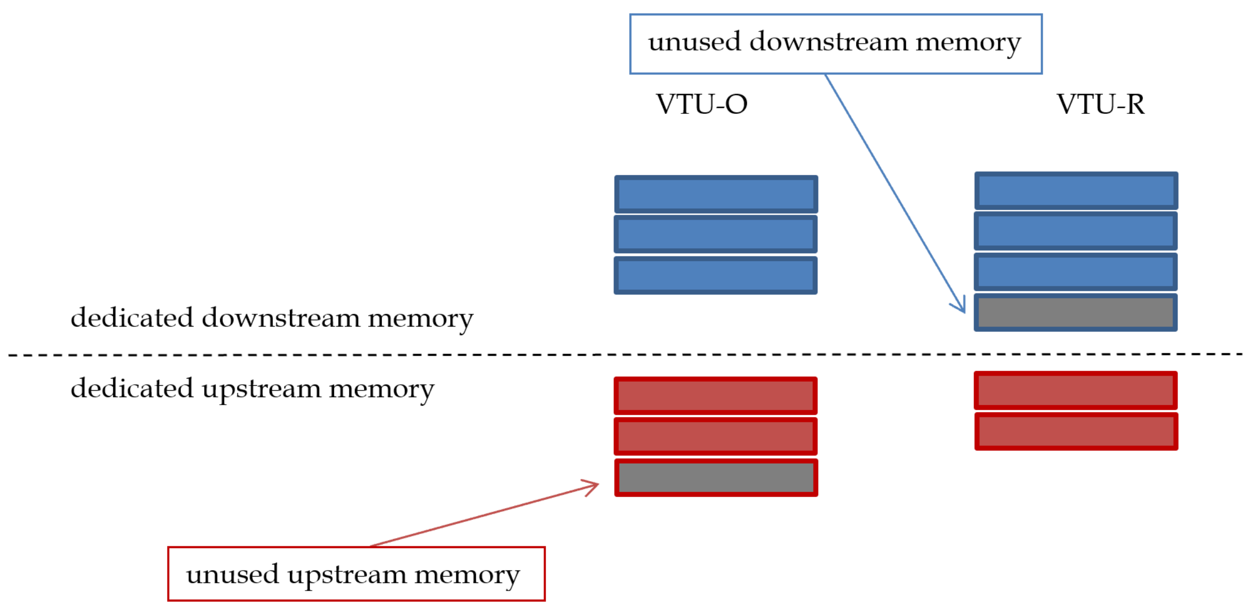

unused memory

Each rectangle represents 10,000 octets of memory.

49. Capabilities (maximum memory supported):



50. Even if each transmitter exchanged their memory capabilities in each direction, the smaller of the transmitter and receiver capabilities in each direction would need to have been chosen. Because the smaller capability is selected, this results in a maximum possible memory allocation as shown below.



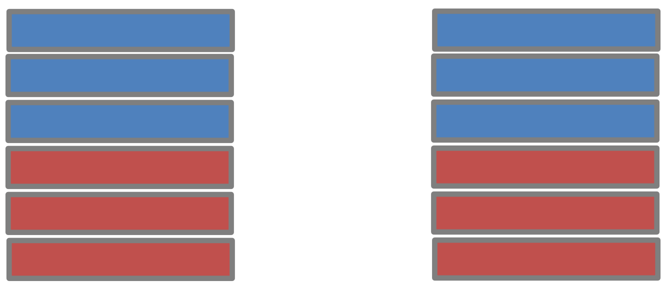
51. Also, because the smaller of the capabilities of the transmitter or receiver are selected in each direction, unused memory for one function in a transceiver cannot be used for another function, e.g., unused dedicated deinterleaver memory in the VTU-R cannot be used for the interleaving function. In the example above, 10,000 octets of deinterleaver memory within the VTU-R and 10,000 octets of deinterleaver memory in the VTU-O would never be used.

52. Under such implementation even though the VTU-R learned about the VTU-O's capabilities downstream, it could not use 10,000 octets of its 40,000 octets of memory that was dedicated to the downstream deinterleaver. Likewise, even though the VTU-O learned about the VTU-R's capabilities upstream, it could not use 10,000 octets of its 30,000 octets of memory that was dedicated to the upstream deinterleaver.

53. In this example, if a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the transceivers would be able to provide that service. If, however, a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the transceivers would NOT be able to meet the requirements of the service.

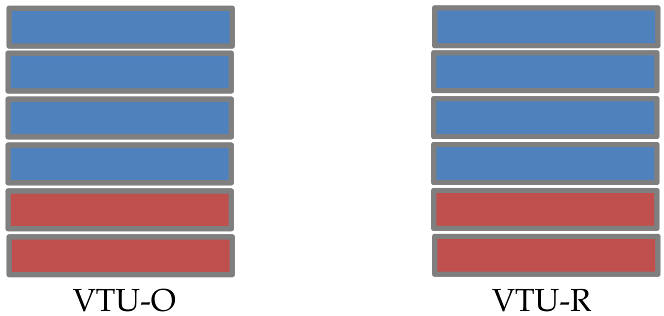
54. The above example can be contrasted with an example implementing the claimed allocation of memory between an interleaving function and a deinterleaving function according to the inventions of the Family 3 patents (Example 2, *infra*).

55. Example 2 (Family 3 Patents). Each transceiver supports a total of 60,000 octets of shared interleaver/deinterleaver memory. If the service provider desires to provide a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 30,000 octets in each transceiver are used for the downstream path and 30,000 octets are used for the upstream path as illustrated below.



VTU-O VTU-R

56. On the other hand, if the service provider desires to provide a VDSL2 service that requires 40,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 40,000 octets in each transceiver are used for the downstream path and 20,000 octets are used for the upstream path as illustrated below.



57. Therefore, unlike the prior art systems where 10,000 octets of memory are unused and the service provider could not provide the service to the customer, when shared memory, which can be allocated between the interleaver function or deinterleaver function, is used, memory that would otherwise go unused can be allocated to one function or the other depending on messages that are, in part, dependent on the service requirements. As illustrated by these examples, the VTU-R is capable of allocating 10,000 octets of its memory to the upstream interleaving function at one time but allocating the same 10,000 octets of its memory to the downstream deinterleaving function at another time. This provides flexibility that enables the transceivers to meet different service requirements.

C. References Cited in Jacobsen Report are Consistent with Implementations that Precede the Inventions of Family 3 Patents

58. Dr. Jacobsen asserts that prior art systems were capable of providing "shared memory that the transceiver can partition between its interleaver and deinterleaver on a per-connection basis. Use of shared memory for interleaving and

deinterleaving, including in DSL, was well known before the priority date of the Family 3 patents." *See* Jacobsen Report at ¶ 72. This is incorrect.

59. To support her argument, Dr. Jacobsen cites to several prior art references. Yet, none of these references discloses what she asserts that they do.

60. Berkmann does not disclose providing "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis," as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. While Berkmann describes using "a combined interleaving and deinterleaving circuit," (*id*. at Abstract), it further explains that "[o]nly the interleaving function α(i) (or, alternatively, the inverse deinterleaving function α^{-1}(i)) must be implemented, but not both functions" (*id*. at ¶ 102). Without much further analysis of Berkmann needed, it is clear that regardless of whether the "combined interleaving and deinterleaving circuit" meets a definition of shared memory as construed by the Court (and it does not), it is not being partitioned ***between*** the interleaving function and the deinterleaving function, and it is not being partitioned on a ***per-connection*** basis. At most, Berkmann discloses a circuit for carrying out interleaving ***or*** deinterleaving, but not both, at the same time, which does not disclose shared memory as construed by the Court.

61. Fadavi-Ardekani does not disclose providing "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis," as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. As explained in, for example, Sections VI.C.1 and VI.C.2, *infra*. Fadavi only teaches that the interleaver and deinterleaver are each provided with a size of memory that "is derived by multiplying the maximum

codeword length by the maximum interleaver depth." Fadavi at 7:9-10. Thus, Fadavi teaches using dedicated memories for the interleaving function and deinterleaving function. Also, as explained in those sections, the disclosed "ping-pang" operation does not meet the shared memory requirement, nor is it the memory assigned on per-connection basis.

62. Kang does not disclose providing "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis," as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72.

63. Mazzoni does not disclose providing "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis," as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. As explained in, for example, Sections VI.B.1, VI.B.3.a, and VI.B.3.b, *infra*, Mazzoni describes the assignment of interleaver memory and deinterleaver memory for predefined data rate pairs (services) by using predefined I and M parameter values for its interleaving means, and predefined I′ and M′ parameter values for deinterleaving means for each data rate pair (i.e., service). *Id.* at 5:24-30. Also, as explained in the cited sections, the assignment is performed at the time of an installation of the modem, and not per-connection basis. *See* Mazzoni at 6:51-61.

64. Voith does not disclose providing "shared memory that can be partitioned between its interleaver and deinterleaver on a per-connection basis," as Dr. Jacobsen asserts. *See* Jacobsen Report at ¶ 72. As explained in Sections VI.E.1 and VI.E.2, *infra*.

Voith merely teaches use of an external memory. Voith does not teach that the external memory is "shared memory."

V. THE ASSERTED CLAIMS OF THE FAMILY 3 PATENTS ARE VALID

65. As set forth in this Rebuttal Report, it is my opinion and conclusion that each Asserted Claim of the Family 3 Patents are not invalid in view of the alleged prior art as asserted in the Jacobsen Report.

66. In performing my analysis, I have compared the limitations of each Asserted Claim with the disclosure in the alleged prior art references. I have also considered the scope and content of the prior art, the differences between the prior art and the claimed invention, the level of ordinary skill in the art at the time of the invention, and whether the differences are such that the claimed invention as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made.

67. In my analysis below, I have applied, where applicable, the Court's claim construction. *See* Cooklev Inf. Report at § X.

A. Claim 19 of the '473 patent is valid under 35 U.S.C. § 112, ¶2

68. Dr. Jacobsen asserts that:

> [C]laim 19 of the '473 patent is indefinite. Claim 19 recites the limitation 'wherein at least a portion of the memory ***may be*** allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.' One of ordinary skill in the art would not have known with reasonable certainty whether a portion of the memory actually has to be allocated to an interleaving function at one time, and a deinterleaving function at another, or whether the mere possibility that some portion of the memory could possibly be allocated to

> the interleaving or deinterleaving function suffices to meet the claim language."

Jacobsen Report at ¶ 151 (emphasis in original).

69. I disagree with Dr. Jacobsen's conclusion as well as with the arguments she presents to support her position as explained below.

70. Dr. Jacobsen's arguments are premised on the assertion that the "Court determined that this language should have its plain meaning during claim construction." Jacobsen Report at ¶ 151. While it is true that the Court gave plain meaning to this claim term, the Court also provided context for this claim language, which Dr. Jacobsen ignores in her analysis. Specifically, the Court noted:

> The claim language does not require that the message specify amounts of memory. The disputed term's language requires that the amount of memory depend on the message's contents, but it does not require that the message's contents themselves actually specify amounts of memory.

Claim Construction Memorandum for Family 3 Patents (Dec. 18, 2017), D.I. 445, ("CC Memo") at p. 10.

71. Dr. Jacobsen ignores the Court's guidance in reaching her conclusion that:

> It is not clear from the intrinsic record, however, whether this allocation actually has to happen, at some point, in order for a device to infringe. For example, a system could use a shared memory in such a way that it is theoretically possible that a portion of the memory is allocated to a deinterleaver or an interleaver, depending on the message, but it might not actually ever happen in practice. One of ordinary skill in the art would not have understood whether such a system would infringe claim 19 of the '473 patent.

Jacobsen Report at ¶ 152.

72. As an initial matter, Dr. Jacobsen refers to the "claims, specification, and file history" as purportedly supporting her unfounded argument. Yet, Dr. Jacobsen

does not explain how either supports her conclusion. In fact, Dr. Jacobsen does not quote from or cite to the claims, specification, or the file history.

73. In any event, Dr. Jacobsen's assertion indicates that she misunderstands the scope of an apparatus claim that defines structure in functional terms. I understand that an apparatus claim is infringed when the accused apparatus is capable of infringement. Therefore, the answer to Dr. Jacobsen's question about the scope of the claim is that the claimed allocation does not actually have to happen in order for the claim to be infringed. Rather, the claim is infringed by transceivers that are capable of allocating at least a portion of the memory to the interleaving function or the deinterleaving function at any one particular time depending on the message.

74. A POSITA would understand that this claim language, as even the Court agreed, requires only that the function to which the portion of memory is allocated at one particular time depends on the message's contents. The use of the term "may" does not render the scope of the claim indefinite. Rather, "may" is the most appropriate term given that the claim provides two possibilities on its face – that, depending on the message, (1) the portion of memory be allocated to the interleaver function at a particular time, or (2) the portion of memory be allocated to the deinterleaver function at a particular time. A transceiver that is not capable of allocating at least some portion of memory to interleaving at one time and allocating that same portion to deinterleaving at another time would not infringe. A transceiver that is capable of doing so, such as the Accused Products, would infringe. Thus, claim 8 9 the '473 patent

informs those skilled in the art about the scope of the invention with reasonable certainty.

75. I note that 2Wire did not raise this indefiniteness argument during claim construction, and in fact proposed a claim construction that literally included the phrase "memory may be allocated." CC Memo at 9-10 (2Wire's proposed construction: "wherein at least a number of bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving /deinterleaving] function at any one particular time depending on the amounts of memory specified in the message."). While I do not agree that 2Wire's proposed claim construction is accurate, 2Wire and Dr. Jacobsen had no problem proposing a construction that included this phrase verbatim. One must assume that 2Wire would not have proposed an indefinite construction for this claim element.

76. For the foregoing reasons, it is my opinion that claim 19 of the '473 patent is definite and that Dr. Jacobsen has not proven otherwise.

B. Written Description and/or Enablement under 35 U.S.C. § 112, ¶1

77. The Court construed the term "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver]" to mean "the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory." Dr. Jacobsen contends

that this term lacks written description and enablement. Jacobsen Report at ¶ 153. I disagree.

78. Dr. Jacobsen acknowledges that "[t]he specification describes sharing resources, such as memory and processing power, as well as ways of allocating those shared resources." Jacobsen Report at ¶ 154. She asserts, however, that the specification purportedly does not "describe or explain how shared memory that is allocated to an interleaver and a deinterleaver can be used at the same time, or even what "used at the same time" even means. As an initial matter, I understand that there is no requirement that the specification describe what "used at the same time means" as long as the plain meaning of the claim language is understood in view of the specification. That is the case here. "Used at the same time" is a common and well understood term in general and one of skill in the art understands what it means to "use" memory. In any event, 2Wire agreed to the Court's construction of this term. CC Memo at p. 9.

79. Further, a POSITA would know how memory that is allocated to two different functions can be "used at the same time." While Dr. Jacobsen asserts that one of skill in the art would not know how this can be done, she does not explain why this is so. In any event, I disagree with her unsupported assertion. The simultaneous use of memory by multiple functions was a well-known process at the time of the inventions. A POSITA at that time would know how two or more functions can simultaneously use the same memory by storing information for a first function at the same time that information for a second function is stored in the memory, or written to the memory, or

read from the memory. This is inherent in any multi-threaded operation that uses the same memory.

80. Dr. Jacobsen asserts that the specification does not explain how memory allocated to an interleaver and memory allocated to a deinterleaver can be used at the same time. I understand that such explanation in the specification is not required. Rather, I understand that a patent need not teach, and preferably omits, what is well known in the art. I also understand that resort to material outside of the specification in order to satisfy the enablement requirement is permissible because it makes no sense to encumber the specification of a patent with all the knowledge of the past concerning how to make and use the claimed invention. Therefore, it was not necessary to provide a full and detailed explanation where, as here, a POSITA would know how to implement the claim.

81. As for Dr. Jacobsen's assertion that there is no written description support for "the shared memory allocated to the [deinterleaver / interleaver] is used at the same time as the shared memory allocated to the [interleaver / deinterleaver], I disagree." 2Wire actually took the opposite position in its claim construction briefing:

> Defendants' proposed construction correctly reflects that the shared memory is read to and written from at the same time by the interleaver and the deinterleaver. Defendants' proposed construction is consistent with the specification, which discloses that "the transmitter and/or receiver latency paths of the transceiver can share an interleaver/deinterleaver memory and the shared memory can be allocated to the interleaver and/or deinterleaver of each latency path."

Parties' Joint Claim Construction Brief for the Family 3 Patents, D.I. No. 353, at p. 58. Additional disclosure that shows that the patent applicant had possession of this

element of the claimed invention at the time the patent application was filed is found at, e.g., U.S. Patent 7,831,890[1] patent at, e.g., Fig. 1 (illustrating shared memory 120 that services at least two interleaving functions and two deinterleaving functions); 6:56-64 and 7:7-25 (explaining that "the transmitter portion and/or receiver portion latency paths would be reconfigured to utilize the shared memory" and describing simultaneous transmitting/encoding and decoding/receiving of the latency paths); 8:11-39 (describing simultaneous use of different portions of a shared memory for various applications).

82. Dr. Jacobsen also asserts that the Family 3 patents lack written description support "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." She does not provide any explanation of why this is so. In any event, I disagree. Disclosure that shows that the patent applicant had possession of this element of the claimed invention at the time the patent application was filed is found generally because the specification discloses the use of "shared memory" by an interleaver and a detinterleaver where the Court interpreted shared memory to mean "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." CC Memo at p. 5. A POSITA would understand from the disclosure of shared memory that the portion of shared memory that is allocated to an interleaver

[1] The '890 patent is the original, non-provisional application in the chain with the asserted Family 3 patents.

would not be used at the same time by a deinterleaver but, instead, could be used at alternative times depending on the allocation in effect at the time.

83. I reserve the right to address any support or explanation Dr. Jacobsen's attempts to provide for her currently conclusory assertions regarding written description and enablement.

84. Based on the foregoing, it is my opinion that the claim 1 of the '048 patent, claim 5 of the '381 patent, and claim 13 of the '882 patent satisfy the written description and enablement requirements.

C. Certificate of Correction

85. I disagree with Dr. Jacobsen's opinion that the "Certificate of Correction changed the scope and meaning of the '381 and '882 patent." Jacobsen Report at ¶ 160. The certificate of correction was properly issued by the patent office to correct obvious typographical errors. Claim 5 of the '381 patent as corrected provides in relevant part:

> 5. A non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver comprising:
>
> allocating, in the transceiver, a first number of bytes of the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission reception at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message;
>
> allocating, in the transceiver, a second number of bytes of the shared memory to an interleaver to interleave a second plurality of RS coded data bytes received transmitted at a second data rate;

86. I have reviewed the specification and it is my opinion that based on the specification, it is clear that the errors were clerical or typographical. Specifically, FIG. 1

of the specification depicts an interleaver as being associated with transmitting and the deinterleaver as being associated with reception. On the other hand, the specification is not consistent with Dr. Jacobsen's hypothetical device that deinterleaves RS coded data bytes before transmitting them and receives RS coded data bytes before interleaving them. Indeed, the best Dr. Jacobsen can say is that the Family 3 patents "do not appear to foreclose either of these possibilities."

87. Dr. Jacobsen's suggests that the statement in the specification that "the invention can be applied to any transceiver having any number of latency paths" somehow precludes the correction. I disagree. That statement merely means that a transmitter of a transceiver can have any number of latency paths and the receiver of the same transceiver can have any number of latency paths. For example, a CO transmitter could have one or two downstream latency paths to the CPE and one or two upstream latency paths from the CPE.

88. Dr. Jacobsen's assertion that "a person of ordinary skill in the art would [not] have considered the terms 'transmission' and 'received' in claim 5 of the '381 patent and claim 13 of the '882 patent to be typographical errors" is not credible, especially so in light of the statements made elsewhere in the Jacobsen Report. For example, at ¶ 55 of the Jacobsen Report, Dr. Jacobsen concedes that "[t]o **apply interleaving**, the transmitter **shuffles consecutive bytes** of the data stream in a known and systematic way **before transmitting them** . . . ." *See also*, Jacobsen Report at ¶ 60 (". . . transmitter interleaves the bytes prior to transmission."). Thus, Dr. Jacobsen recognizes that bytes are interleaved prior to being "transmitted." Dr. Jacobsen also

admits that "the receiver . . . can reverse the interleaving process by collecting all of the interleaving data elements and using a complementary deinterleaving process." Jacobsen Report at ¶ 58. Thus, Dr. Jacobsen recognizes that bytes are deinterleaved after "reception."

89. Accordingly, her assertion that the errors were not typographical (or that they would not have been recognized as typographical) is meritless.

VI. ANALYSIS OF THE CITED REFERENCES

A. The Asserted Claims Are Not Obvious Over LB-031

90. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of the Asserted Claims, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

91. It is also my opinion that regardless of the disclosure of LB-031 and the other cited references, a person of ordinary skill in the art would not be motivated to combine the teachings of LB-031 with the teachings of the other cited references at least for the reasons described in Section VI.A.2, *infra*.

1. Overview of LB-031

92. LB-031 focuses on defining an interleaver delay in units of time to allow reduced interleaver complexity at lower data rates. *See* LB-031 at 3 (2WIRE00030959) ("Therefore, it seems prudent to define the interleaver complexity requirements in a way that will allow those who want to deploy VDSL2 at lower speeds to do so at a reduced complexity with respect to higher speed implementations. The way to do this

and to guarantee some minimum level of performance is to specify the interleaver complexity in terms of the delay in time.").

93. LB-031 notes that the delay in time is proportional to the interleaver depth and to the codeword size and inversely proportional to the data rate. *Id*.

94. LB-031 describes memory requirements for an "interleaver/deinterleaver pair." *See, e.g.*, LB-031 at 2 (2WIRE00030958) ("The smallest amount of memory required to build an interleaver/deinterleaver pair is equal to the total delay of the interleaver/deinterleaver. Typically, for memory optimized interleavers, the interleaver and deinterleaver memory size is nearly the same."). *See also* § VI.A.2, *infra*. The interleaver of this "pair" is located in the transmitter lineup of one transceiver, while the deinterleaver of the "pair" is located in the receiver lineup of the other transceiver. The "pair" are associated with a single latency path and direction, i.e., a single path in the upstream direction or a single path in the downstream direction.

95. While LB-031 acknowledges that "[t]he size of the interleaver memory will be a major source of complexity in VDSL2," it does not describe the combined memory requirements of an interleaver associated with one direction (e.g., upstream) and deinterleaver associated with the other direction (e.g., downstream) within a single transceiver. Nor does it describe sharing a memory between an interleaver and deinterleaver in a single transceiver as called for by the Asserted Claims of the Family 3 Patents and as described in more detail in VI.A.1, *supra*. Instead, LB-031 focuses on selecting an amount of interleaver or deinterleaver memory for a single direction (i.e., by comparing capabilities of the transmitter on one end of a communication channel

with the capabilities of the receiver on the other end). *See, e.g.*, LB-031 at 3 (2WIRE00030959). The relevant portion of LB-031 is quoted below:

> For interoperability reasons, the VTU-O and VTU-R must exchange the interleaver delay in terms of octets. The requirement is that the interleaver delay in octets be sufficient to satisfy the smallest maximum delay even at the highest supported data rate. If a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value. The VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end capabilities.

Id.

96. Contrary to Dr. Jacobsen's opinion, there is nothing in LB-031 that would suggest to a POSITA that a memory is being shared, or should be shared, between an interleaver and a deinterleaver in a single transceiver.

97. At least for these reasons, and for the reasons described in detail below, it is my opinion and conclusion that LB-031 fails to disclose or suggest all element of the Asserted Claims, and hence fails to render the Asserted Claims obvious.

2. LB-031 Does Not Render Claim 1 of the '048 Patent Obvious

98. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 1 of the '048 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a system that allocates shared memory.

99. Contrary to Dr. Jacobsen's assertion, the LB-031 reference does not disclose a system that allocates shared memory. *See* Jacobsen Report at ¶¶ 179-181. Dr. Jacobsen has not pointed to any portion of LB-031 that states, or that would have

disclosed to a POSITA that a transceiver implementing the LB-031 reference allocates shared memory.

100. Dr. Jacobsen points to Eq. 1 and Eq. 5, and corresponding descriptions in the LB-031 reference to assert that a POSITA "would have understood this example to teach allocating memory for interleaving and deinterleaving." *See* Jacobsen Report at ¶ 180. As an initial matter, this statement is vague because it is not clear whether it is intended to describe the memory of a single transceiver or, on the other hand, the separate memories of a respective interleaver in one transceiver and corresponding deinterleaver in a second transceiver. To the extent she intends the latter, such teaching is not relevant to any asserted claim of the Family 3 patents because the claims are directed to allocating a shared memory between and interleaver and deinterleaver within a single transceiver. To the extent she intends the former, her statement is incorrect.

101. The disclosure of LB-031 Dr. Jacobsen relies on for purportedly disclosing allocating a shared memory is the passage on page 4 of LB-031, which states "[i]f the minimum interleaver delay requirement were 5.23 ms, then, from equation (5) and equation (1), this transceiver must support a delay of at least 29092 octets which corresponds to having an interleaver memory of at least 14546 octets according to equation (2)." *See* Jacobsen Report at ¶ 180. This discussion in LB-031, however, has nothing to do with sharing memory or allocating a shared memory. Rather, it is describing the memory requirements for an interleaver in one transceiver and the corresponding memory requirements for a deinterleaver in a second transceiver at the

other end of the communication channel. As the reference discloses, for an end-to-end delay of 29092 octets, the interleaver memory in one transceiver would have to be 14546 octets (i.e., bytes). The deinterleaver memory for the corresponding deinterleaver in the transceiver at the other end of the communication channel would also be 14546. The memory requirements are the same for the interleaver and corresponding deinterleaver because the deinterleaver will deinterleave the interleaved byte stream that was interleaved by the interleaver.

102. Yet, Dr. Jacobsen omits the fact that the equations of LB-031 are to be used to separately characterize the delay and memory requirements for a single latency path/direction. *See id*. These equations do not characterize the combined memory requirements for a single transceiver that requires memory for an interleaver for a first latency path/direction and a deinterleaver for a second latency path/direction. The equations are not concerned with the combined memory limit of any single transceiver or with sharing or allocating that combined limit between and interleaver and a deinterleaver. Rather, LB-031 is perfectly consistent with the practice at the time of using a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory within a transceiver. As explained in Section VI.A.1, *supra*, LB-031 falls within the category of dedicated interleaver and deinterleaver memory implementations.

103. I note that Dr. Jacobsen understands that DSL transceivers generally transmit/interleave in one direction while they are receiving/deinterleaving in the

other direction.[2] *See, e.g.*, ¶ 207 ("VDSL transceivers transmit and receive data at the same time (i.e., VTU-O transmits data downstream and receives data upstream at the same time, and the VTU-R transmits data upstream and receives data downstream at the same time."). She ignores or attempts to confuse this fundamental detail, however, when comparing the preamble (and notably all the other elements of the claims, except the last) to the LB-031 reference.

104. The claim construction of the term "shared memory" further supports the fact that LB-031 does not disclose shared memory, or allocating shared and consequently does not disclose a system for allocating shared memory. Specifically, the Court construed "shared memory" to mean "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." Claim Construction Order for Family 3 Patents (December 28, 2017) ("CC Order") at p. 2.

105. The second portion of the construction (i.e., that "a portion of [the shared] memory can be used by either function") means that the shared memory is a memory of a single transceiver. For example, the two functions in the context of the claim (and in the context of the asserted claims of the Family 3 patents generally) are interleaving and deinterleaving. The concept of use of a portion of memory by either one function or the other function has been described in Section VI.A.5.b, *infra*. As discussed in connection with the '473 patent, *infra*, the interleaving function and corresponding deinterleaving

[2] This is not the case, however, when the transceiver provides only half-duplex communications, i.e., the transceiver transmits but does not receive at some times and receives but does not transmit at other times.

function of the other transceiver specifically discussed in LB-031 use entirely different memories in different transceivers. No portion of memory within a single transceiver is disclosed by LB-031 to be used by an interleaver at one time or a deinterleaver at another time. *See* § VI.A.5.a.

106. Second, Dr. Jacobsen inappropriately extends the actual disclosure and teachings of the LB-031 reference by making an inherency argument that contradicts her other arguments. *See* Jacobsen Report at ¶ 181. Dr. Jacobsen asserts that "one of ordinary skill in the art would have understood from the disclosures of LB-031 that the allocated memory can be a shared memory." *See id*. This is incorrect. First, Dr. Jacobsen has not identified any disclosure in LB-031 that requires that a shared memory is used or that any portion of memory within a single transceiver can be used by the interleaver or the deinterleaver. Rather, again, LB-031 is perfectly consistent with the practice of its time, which was to use a dedicated, fixed-size interleaver memory and a separate, dedicated, fixed-size deinterleaver memory in a transceiver. *See* § VI.A.5.a, *infra*; *see also* § IV.A, and IV.B, *supra*. Thus, no portion of a memory can be used by either an interleaver or a deinterleaver (i.e., no portion of the dedicated interleaver memory will ever be used by the deinterleaver and no portion of the dedicated deinterleaver memory will ever be used by the interleaver.).

107. Further, Dr. Jacobsen recognizes that LB-031 explains that "[t]he size of the interleaver memory will be a major source of complexity in VDSL2." *See* Jacobsen Report at ¶ 181 (citing LB-031 at 3.). This statement does not state or suggest that size or complexity can be reduced by sharing memory. Rather, this statement would

discourage a POSITA from attempting to add further complexity to interleaver memory in VDSL2, such as by proposing a memory sharing scheme. *See also, e.g.*, LB-031 at 3 (2WIRE00030959) ("Therefore, it seems prudent to define interleaver complexity requirement in a way that will allow those who want to deploy VDSL2 at lower speeds to do so that at a reduced complexity with respect to higher speed implementations.").

108. Therefore, I do not agree that a POSITA would understand "from the disclosures of LB-031 that the allocated memory can be a shared memory," as Dr. Jacobsen incorrectly asserts, because a shared memory implementation would increase and not decrease the complexity of the implementation proposed by the LB-031 reference. *See* Jacobsen Report at ¶ 181.

109. I also disagree with Dr. Jacobsen's assertion that "it was well known by the priority date of the Family 3 patents that an interleaver and deinterleaver memory could share a memory." *See* Jacobsen Report at ¶ 181. I address this in Sections IV.A, IV.B, and IV.C, *supra.* Additionally, and *arguendo*, even if any of the string-cited references in paragraph 182 of the Jacobsen Report disclose a system for sharing memory as construed by the Court (which they do not), Dr. Jacobsen fails to explain why a POSITA would look to any of these references to increase complexity of the implementation of the LB-031 disclosure. Rather, as I have explained immediately above, a POSITA would be discouraged from adding complexity to the memory requirement specifying scheme of LB-031. Consequently, there would be no motivation to combine any of the references cited in Paragraphs 182 of the Jacobsen Report with LB-031. And Dr. Jacobsen supplies none.

110. Because the LB-031 reference does not disclose, teach, or suggest a system that allocates sheared memory, it does not render claim 1 of the '048 patent anticipated or obvious. Also, because a person of ordinary skill in the art would not have understood from the teaching of the LB-031 reference to require a use of a shared memory, the LB-031 reference does not render claim 1 of the '048 patent anticipated or obvious. Finally, because a person of the ordinary sill in the art would not be motivated to combine the teaching of the LB-031 reference with the teaching of any other references cited by Dr. Jacobsen, and in fact, would be discouraged to do so, the LB-031 reference in combination with any of those references or in combination with the knowledge of one of ordinary skill in the art at the time of the invention of the Family 3 patents, does not render claim 1 of the '048 patent obvious.

b. LB-031 does not disclose determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

111. LB-031 does not disclose this claim element.

112. Dr. Jacobsen ignores the requirement of this claim element that calls for a "shared memory" and instead irrelevantly quotes the portions of LB-031 describing the memory requirements for an interleaver in one transceiver and a corresponding memory requirement for a deinterleaver in another transceiver (and not an implementation in a single transceiver with a shared memory). *See* Jacobsen Report at ¶ 192.

113. At least because LB-031 is not directed to allocating shared memory described in § 90 and § 98, *supra*, the LB-031 reference does not disclose, teach, or suggest this claim element. *See* § VI.A.5.a, *infra*; *see also* § IV.A, and IV.B, *supra*.

114. Because LB-031 does not disclose, teach, or suggest determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory, it does not render claim 1 of the '048 Patent obvious.

c. LB-031 does not disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

115. LB-031 does not disclose, teach, or suggest this claim element.

116. As with the previous claim element, Dr. Jacobsen yet again ignores the requirement of this claim element that calls for a "shared memory." *See* Jacobsen Report at ¶¶ 194-195. The claim overall, and also this element in particular, calls for allocating bytes of a shared memory. LB-031 lacks disclosure of a shared memory as construed by the Court. *See* §§ VI.A.1, VI.A.2.a. *See also* § VI.A.5.a, *infra*; *see also* § IV.A, and IV.B, *supra*.

117. Dr. Jacobsen relies on a passage from LB-031 describing an exchange between a VTU-O and VTU-R of capabilities (i.e., a VTU-R and VTU-O will select "the smaller of the transceivers and receiver capabilities in each direction."). But the implementation details are all described in the context of the interleaver/deinterleaver pair for a single direction, e.g., interleaver capabilities of the VTU-O and deinterleaver

capabilities of the VTU-R for the downstream direction. While the exchange of capabilities allows the transceivers to use only up to the amount of memory that is the lesser of the amount of interleaver memory in the VTU-O or the amount of deinterleaver memory in the VTU-R, there is no contemplation or discussion of sharing memory within a single transceiver depending on the exchanged capabilities. Thus, Dr. Jacobsen's conclusion that a "shared memory" is being allocated is not supported by the LB-031 reference. *See* Jacobsen Report at ¶ 194; *see also* LB-031 at 2 (2WIRE00030958). Again, as explained in §§ VI.A.1, VI.A.2.a, *supra*, the disclosure of the LB-031 reference is not directed to shared memory. *See also* § VI.A.5.a, *infra*; *see also* § IV.A, and IV.B, *supra*.

118. Because LB-031 does not disclose, teach, or suggest allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, it does not render claim 1 of the '048 Patent obvious.

d. LB-031 does not disclose wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message.

119. LB-031 does not disclose this limitation at least because, as I explain in Section VI.A.2.a, *supra*, it does not disclose allocating memory to an interleaver (or a deinterleaver.)

120. Because LB-031 does not disclose, teach, or suggest transmitting or receiving a message during initialization specifying a maximum number of bytes of

memory that are available to be allocated to an interleaver, it does not render claim 1 of the '048 patent obvious.

e. LB-031 does not disclose allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate.

121. LB-031 does not disclose, teach, or suggest this claim element.

122. Dr. Jacobsen makes the same arguments for this claim element as for the previous element, all of which have been addressed in § VI.A.2.c, *supra* and are incorporated by reference with respect to this claim element.

123. As with the previous element, LB-031 lacks disclosure of shared memory as construed by the Court. Therefore, LB-031 cannot disclose or suggest this claim element. *See* §§ VI.A.1, VI.A.2.a; *see also* § VI.A.5.a, *infra* and §§ IV.A and IV.B, *supra*.

124. Again, the implementation details of LB-031 are all described in the context of the interleaver/deinterleaver pair for a single direction, e.g., interleaver capabilities of the VTU-O and deinterleaver capabilities of the VTU-R for the downstream direction. There is no disclosure or contemplation of sharing a memory within a single transceiver for an interleaver operating in a first direction and a deinterleaver operating in a second direction. Thus, even assuming, *arguendo*, that LB-031 discloses "allocating a first number of bytes of" a non-shared memory "to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate," there is no disclosure or contemplation of "allocating a second number of bytes of" the same memory "to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate." The

deinterleaving of "a second plurality of RS coded data bytes received at a second data rate" recited in the claim is necessarily referring to communications made in the other direction. LB-031 does not describe sharing memory between an interleaver for one direction and a deinterleaver for the other direction.

125. Because LB-031 does not disclose, teach, or suggest allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received a second data rate, it does not render claim 1 of the '048 Patent obvious.

f. LB-031 does not disclose interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver.

126. LB-031 does not disclose, teach, or suggest this claim element.

127. Dr. Jacobsen makes the same arguments for this claim element as for the previous element, all of which have been addressed in § VI.A.2.c, *supra* and are incorporated by reference with respect to this claim element.

128. As with the previous elements, LB-031 lacks disclosure of shared memory as construed by the Court. Again, LB-031 is consistent with the practice at that time of using a dedicated interleaver memory and a separate deinterleaver memory. Thus, LB-031 does not describe interleaving and deinterleaving within a shared memory as required by this claim element. *See* §§ VI.A.1, VI.A.2.a; *see also* § VI.A.5.a, *infra* and §§ IV.A and IV.B, *supra*.

129. Dr. Jacobsen again ignores the requirement that the memory be shared within a single transceiver as required by this claim as further supported by the Court's construction of the term. Notably, Dr. Jacobsen does not cite to a specific portion of LB-031 refence to support its conclusion that a single transceiver would interlevel and deinterleave within a shared memory. *See* Jacobsen Report at ¶ 205. Instead, Dr. Jacobsen repeats the claim element and jumps to an unsupported conclusion that it is met by LB-031.

130. Because LB-031 does not disclose, teach, or suggest interleaving the first plurality of RS coded data bytes within the shared memory allocated to the interleaver and deinterleaving the second plurality of RS coded data bytes within the shared memory allocated to the deinterleaver, it does not render claim 1 of the '048 Patent obvious.

g. LB-031 does not disclose wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver.

131. LB-031 does not disclose, teach, or suggest this claim element.

132. As discussed in Sections VI.A.1, VI.A.2.a, VI.A.3.c, VI.A.3.d, *supra*, and in Section VI.A.5.a, *infra*, LB-031 does not disclose allocating shared memory in a single transceiver. At least because of the lack of disclosure directed to shared memory and to allocation of such memory, LB-031 does not disclose, teach, or suggest this claim element.

133. Dr. Jacobsen argues that because a transceiver can transmit and receive at the same time, this element is met. *See* Jacobsen Report at ¶ 207. When making this

conclusory argument, Dr. Jacobsen overlooks the fact that the allocated memory refers to memory that can be allocated to an interleaver or a deinterleaver of a single transceiver as discussed in Sections VI.A.1, VI.A.2.a, VI.A.3.b, VI.A.3.d, *supra*. *See also* § VI.A.5.a.

134. At least because LB-031 does not disclose the claimed allocation of memory as discussed in, for example, Sections VI.A.3.c, VI.A.3.d, *supra*, LB-031 cannot disclose or suggest this element of claim 1 of the '048 patent.

135. Because LB-031 does not disclose, teach, or suggest wherein the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver, it does not render claim 1 of the '048 Patent obvious.

3. LB-031 Does Not Render Claim 5 of the '381 Patent Obvious

136. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 5 of the '381 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver.

137. LB-031 describes a prior art system that is not related to sharing memory in a transceiver. *See generally* § VI.A.1, *supra*.

138. As described in Section VI.A.2.a, LB-031 does not include any disclosure directed to allocating shared memory in a transceiver. Consequently, for the same

reasons as described with respect to claim 1 of the '048 patent, LB-031 fails to disclose this element of claim 5 of the '381 patent.

139. Additionally, Dr. Jacobsen does not identify any portions of LB-031 that disclose a non-transitory computer-readable information storage media having stored thereon instruction that are executed by a processor. *See* Jacobsen Report at ¶ 210. Instead, Dr. Jacobsen without any support simply draws an inference that "[o]ne of ordinary skill in the art would have understood that a source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor." *See id*.

140. First of all, Dr. Jacobsen's conclusion is wrong on its face. Source code (or object code) cannot be executed by a processor. A POSITA would understand that source code (or object code) is a term of art referring to uncompiled and non-executable human readable code.

141. Even ignoring the fact that Dr. Jacobsen's conclusion is wrong on its face, Dr. Jacobsen did not show that any element of claim 5 of the '381 patent is performed by executing instructions stored on a non-transitory computer-readable information media. A POSITA would understand that it is possible that one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media. Dr. Jacobsen did not even attempt to show one way or another with which of these possibilities LB-031 would be concerned with respect to each claimed function.

142. It is my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 5 of the '381 patent and therefore fails to render claim 5 of the '381 Patent obvious.

b. LB-031 does not disclose determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

143. LB-031 does not disclose, teach, or suggest this claim element.

144. Dr. Jacobsen incorporates her arguments from Section IX.A.3.d of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.b with respect to claim 1 of the '048 patent.

145. Because LB-031 does not disclose, teach, or suggest determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory, it does not render claim 5 of the '381 Patent obvious.

c. LB-031 does not disclose allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

146. LB-031 does not disclose allocating, at the transceiver, a first number of bytes of shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate.

147. LB-031 does not disclose, teach, or suggest this claim element.

148. Dr. Jacobsen incorporates her arguments from Section IX.A.3.e of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.c with respect to claim 1 of the '048 patent and with respect to an interleaver.

149. Additionally, Dr. Jacobsen incorporates her arguments from Section IX.A.3.g of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.e with respect to claim 1 of the '048 patent and with respect to a deinterleaver.

150. Because LB-031 does not disclose, teach, or suggest allocating, at the transceiver, a first number of bytes of shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, it does not render claim 5 of the '381 Patent obvious.

d. LB-031 does not disclose wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes in the message.

151. LB-031 does not disclose this limitation at least because, as I explain in Section VI.A.2.a, *supra*, it does not disclose allocating memory to an interleaver (or a deinterleaver.)

152. Dr. Jacobsen incorporates her arguments from Section IX.A.3.f of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.d with respect to claim 1 of the '048 patent. Although, claim 1 of the '048 is directed to "allocated memory for the interleaver," my arguments hold true for "allocated memory for the deinterleaver," as recited in claim 5 of the '381 patent, at least because LB-031d does not disclose a system for allocating memory to an interleaver or to a deinterleaver. *See, e.g.*, §VI.A.2.a.

153. Because LB-031 does not disclose, teach, or suggest transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver, it does not render claim 5 of the '381 patent obvious.

e. LB-031 does not disclose allocating, at the transceiver, a second number of bytes of shared memory to an interleaver to interleave a second plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate.

154. LB-031 does not disclose, teach, or suggest this claim element.

155. Dr. Jacobsen incorporates her arguments from Section IX.A.3.e of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.c with respect to claim 1 of the '048 patent and with respect to an interleaver.

156. Additionally, Dr. Jacobsen incorporates her arguments from Section IX.A.3.g of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.e with respect to claim 1 of the '048 patent and with respect to a deinterleaver.

157. Because LB-031 does not disclose, teach, or suggest allocating, at the transceiver, a second number of bytes of shared memory to an interleaver to interleave a second plurality of Reed Solomon (RS) coded data bytes for transmission at a second data rate, it does not render claim 5 of the '381 Patent obvious.

f. LB-031 does not disclose deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and intervening the second plurality of RS coded data bytes within the shared memory allocated to the interleaver.

158. LB-031 does not disclose, teach, or suggest this claim element.

159. Dr. Jacobsen incorporates her arguments from Section IX.A.3.h of the Jacobsen Report, which have been addressed *supra* in Section VI.A.2.f with respect to claim 1 of the '048 patent. The difference in wording of this claim element as compared with the corresponding claim element of claim 1 of the '048 is of no consequence to my arguments.

160. Because LB-031 does not disclose, teach, or suggest deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and intervening the second plurality of RS coded data bytes within the shared memory allocated to the interleaver., it does not render claim 5 of the '381 Patent obvious.

g. LB-031 does not disclose wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver.

161. LB-031 does not disclose, teach, or suggest this claim element.

162. Dr. Jacobsen incorporates her arguments from Section IX.A.3.i of the Jacobsen Report, which have been addressed *supra* in Section VI.A.3.g with respect to claim 1 of the '048 patent. The difference in wording of this claim element as compared with the corresponding claim element of claim 1 of the '048 is of no consequence to my arguments.

163. Because LB-031 does not disclose, teach, or suggest deinterleaving the first plurality of RS coded data bytes within the shared memory allocated to the deinterleaver and intervening the second plurality of RS coded data bytes within the

shared memory allocated to the interleaver., it does not render claim 5 of the '381 Patent obvious.

4. LB-031 Does Not Render Claim 13 of the '882 Patent Obvious

164. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 13 of the '882 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a system that allocates shared memory.

165. LB-031 does not disclose, teach, or suggest this claim element of claim 13 of the '882 Patent for the same reason as discussed with respect to the same claim element of claim 1 of the '048 Patent. *See* § VI.A.2.a.

b. LB-031 does not disclose other elements of this claim.

166. Dr. Jacobsen adopts wholesale her arguments with respect to claim 5 of the of the '381 patent (elements 5[b] – 5[h]) as her argument with respect to claim 13 of the '882 patent (elements 13[c] through 13[i], respectively). *See* Jacobsen Report at ¶ 232.

167. Accordingly, I hereby incorporate my arguments with respect to claim elements of claim 5 of the '381 patent, and also claim 1 of the '048 Patent as rebuttal augment for the respective claim elements of claim 13 of the '882 patent.

168. Specifically, using the claim element numbering from Dr. Jacobsen Report (*see* Appendix C to Jacobsen Report), I hereby incorporate herein the following sections of this report:

- with respect to element 13[d], I incorporate §§ VI.A.2.b, VI.A.3.b, *supra*;

- with respect to element 13[e], I incorporate §§ VI.A.2.c, VI.A.3.c, *supra*;
- with respect to element 13[f], I incorporate §§ 116, VI.A.3.d, *supra*;
- with respect to element 13[g], I incorporate §§ VI.A.2.e, VI.A.3.e, *supra*;
- with respect to element 13[h], I incorporate §§ VI.A.2.f, VI.A.3.f, *supra*;
- with respect to element 13[i], I incorporate §§ VI.A.2.g, VI.A.3.g, *supra*.

169. LB-031 does not disclose, teach, or suggest the above claim elements of claim 13 of the '882 Patent for the same reason as discussed with respect to the substantially similar claim elements of claim 5 of the '381 Patent, and claim 1 of the '048 Patent.

5. LB-031 Does Not Render Claim 19 of the '473 Patent Obvious

170. It is my opinion and conclusion that LB-031 alone or in combination with other cited references fails to disclose or suggest each element of claim 19 of the '473 patent, and hence fails to render the Asserted Claims anticipated or obvious as described in detail, below.

a. LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver.

i. LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function.

171. LB-031 does not disclose, teach, or suggest a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during

initialization of the transceiver. As discussed in the Overview of LB-031 Section, *supra*, and also in connection with claim 1 of the '048 patent, *supra*, LB-031 does not disclose allocating a memory between an interleaver function and a deinterleaver function in a single transceiver but instead discloses exchanging "capability" information specifying the size of a dedicated interleaver memory and the size of a separate, dedicated deinterleaver memory. *See* § 90; *see also* § VI.A.2.a.

172. No portion of any memory contemplated by LB-031 is used as interleaver memory at one point in time and deinterleaver memory at another point in time and, thus, LB-031 does not allocate memory *between* an interleaving function and a deinterleaving function. Rather, one of ordinary skill in the art would understand LB-031 in the context of a system in which the CO transceiver (VTU-O) has a dedicated amount of memory available to be used for downstream interleaving and a separate, dedicated amount of memory available to be used for upstream deinterleaving and the CPE transceiver (VTU-R) has a dedicated amount of memory available to be used for downstream deinterleaving and a separate, dedicated amount of memory available to be used for upstream interleaving. In the VTU-O, no portion of the dedicated downstream interleaver memory can be allocated for upstream deinterleaving and, no portion of the upstream deinterleaver memory can be allocated for downstream interleaving. Likewise, in the VTU-R, no portion of the dedicated upstream interleaver memory can be allocated for downstream deinterleaving and, no portion of the downstream deinterleaver memory can be allocated for upstream interleaving.

173. Dr. Jacobsen describes the disclosure in LB-031 of transceivers exchanging capabilities, including specifying the amount of memory a transceiver has available for a particular latency path by exchanging the end-to-end interleaver delay on octets that it can support for that latency path. *See* Jacobsen Report at ¶¶ 242-244. She refers to the disclosure in LB-031 that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," in which case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities." *See* Jacobsen Report at ¶ 243 (citing LB-031 at 3). But this is merely standard behavior for DSL transceivers at that time. Dr. Jacobsen does not point to any disclosure in LB-031 where memory is allocated between an interleaving function and a deinterleaving function in accordance with a message. Further explanation of the distinctions between LB-031 and claim 19 of the '473 patent is provided below.

ii. LB-031 does not disclose the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during initialization of the transceiver.

174. Even assuming that the exchange of information described in LB-031 occurs during initialization and occurs through an exchange of messages, LB-031 would not disclose to a person of ordinary skill in the art a message that is used to perform the claimed allocation. In particular, LB-031 discloses that "[i]f a VDSL2 implementation supports a larger interleaver memory than is required, it should be free to specify the larger value," and that in such a case "[t]he VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities, in each direction, as the end-to-end

capabilities." LB-031 at 3. This disclosure would be understood by a POSITA as follows:

<u>For determining capabilities applicable to the downstream (DS) direction (i.e., downstream latency path from VTU-O to VTU-R):</u>

> Step 1. The VTU-O sends a message to the VTU-R that includes the amount (in octets) of downstream interleaver delay that the VTU-O can support ("Message 1-DS").
>
> Step 2. The VTU-R sends a message to the VTU-O that includes the amount (in octets) of downstream deinterleaver delay that the VTU-R can support ("Message 2-DS").
>
> Step 3. For the downstream deinterleaver delay capabilities, the VTU-R would select the smaller of the downstream interleaver delay amount indicated in Message 1-DS and the downstream deinterleaver delay amount indicated in Message 2-DS.
>
> Step 4. Separately, for the downstream interleaver delay capabilities, the VTU-O would select the smaller of the downstream interleaver delay amount indicated in Message 1-DS and the downstream deinterleaver delay amount indicated in Message 2-DS.
>
> (Step 4 may not be necessary because it will ultimately be up to the VTU-R to determine the amount of delay actually implemented for the downstream path.)

<u>For determining capabilities applicable to the upstream (US) direction (i.e., upstream latency path from VTU-R to VTU-O):</u>

> Step 1. The VTU-O sends a message to the VTU-R that includes the amount (in octets) of upstream deinterleaver delay that the VTU-O can support ("Message 1-US").
>
> Step 2. The VTU-R sends a message to the VTU-O that includes the amount (in octets) of upstream interleaver delay that the VTU-R can support ("Message 2-US").
>
> Step 3. For the upstream deinterleaver delay capabilities, the VTU-O would select the smaller of the upstream deinterleaver delay amount indicated in Message 1-US and the upstream interleaver delay amount indicated in Message 2-US.

Step 4. Separately, for the upstream interleaver delay capabilities, the VTU-R would select the smaller of the upstream deinterleaver delay amount indicated in Message 1-US and the upstream interleaver delay amount indicated in Message 2-US.

(Step 4 may not be necessary because it will ultimately be up to the VTU-O to determine the amount of delay actually implemented for the upstream path.)

175. In the examples above, a single message from the VTU-O to the VTU-R could include the Message 1-DS and Message 1-US capabilities information and a single message from the VTU-R to the VTU-O could include the Message 2-DS and Message 2-US capabilities information. But, again, even if a POSITA would understand there to be a message exchange such as the example described above, no portion of memory is allocated between the interleaving function and the deinterleaving function in accordance with a message.

176. Instead, LB-031 at most discloses that, for the downstream direction, a VTU-R with a larger dedicated deinterleaver memory than is required can determine whether the VTU-O also supports a larger amount. But, if the VTU-O does not support a larger amount than is required, however, the extra deinterleaver memory of the VTU-R is simply not used. For example, it is not available to be used for the upstream interleaver function. The examples described below illustrate this concept.

177. Example 1. VTU-O (30,000 octets of dedicated downstream interleaver memory; 30,000 octets of dedicated upstream deinterleaver memory). VTU-R (40,000 octets of dedicated downstream deinterleaver memory; 20,000 octets of dedicated upstream interleaver memory).

Legend:

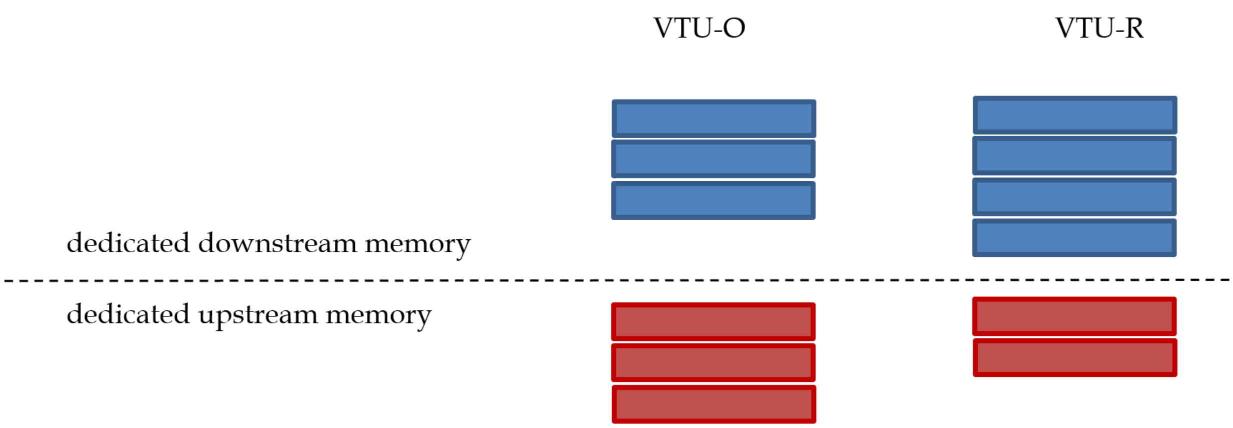
dedicated downstream memory (interleaver memory for VTU-O, deinterleaver memory for VTU-R)

dedicated upstream memory (interleaver memory for VTU-R, deinterleaver memory for VTU-O)

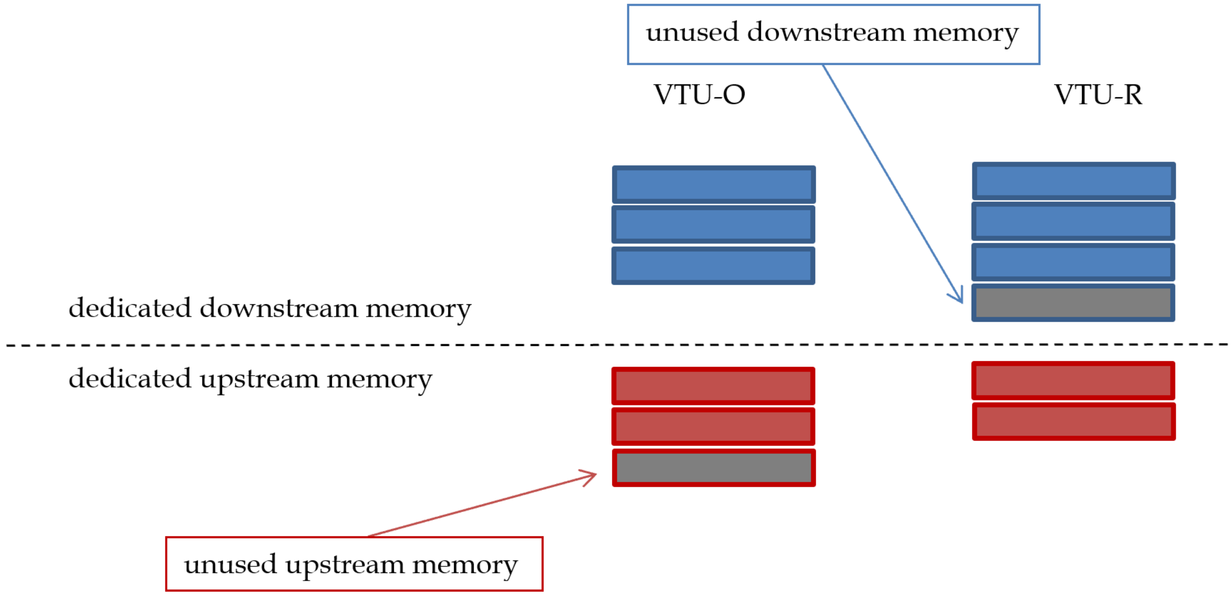
unused memory

Each rectangle represents 10,000 octets of memory.

178. Capabilities (maximum memory supported):



179. According to LB-031, each transmitter would exchange their memory capabilities in each direction and "then select the smaller of the transmitter and receiver capabilities, ***in each direction***." Consistent with the state of art of its time, LB-031 teaches that the smaller capability is selected. Because the smaller capability is selected, this results in a maximum possible memory allocation as shown below.



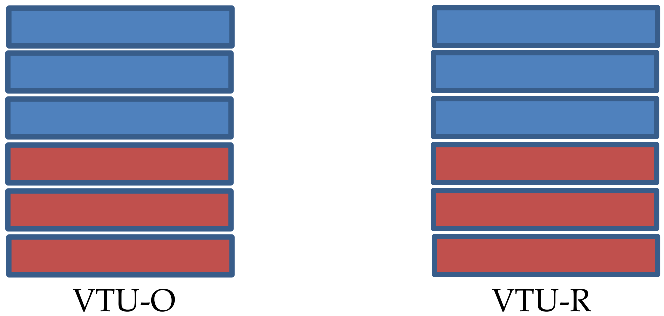
180. Because the smaller of the capabilities of the transmitter or receiver are selected in each direction in accordance with the express teaching of LB-031, unused memory for one function in a transceiver cannot be used for another function, e.g., unused dedicated deinterleaver memory in the VTU-R cannot be used for the interleaving function. In the example above, 10,000 octets of deinterleaver memory within the VTU-R and 10,000 octets of deinterleaver memory in the VTU-O would never be used.

181. Under the LB-031 implementation even though the VTU-R learned about the VTU-O's capabilities downstream, it could not use 10,000 octets of its 40,000 octets of memory that was dedicated to the downstream deinterleaver. Likewise, even though the VTU-O learned about the VTU-R's capabilities upstream, it could not use 10,000 octets of its 30,000 octets of memory that was dedicated to the upstream deinterleaver.

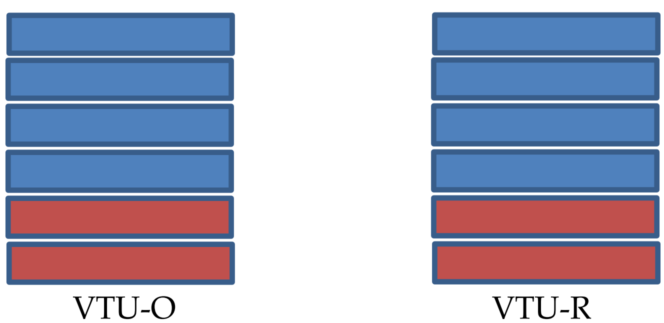
182. In this example, if a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the transceivers would be able to provide that service. If, however, a service provider is providing a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the transceivers would NOT be able to meet the requirements of the service.

183. The above example can be contrasted with an example implementing the claimed allocation of memory between an interleaving function and a deinterleaving function according to the inventions of the Family 3 patents (Example 2, *infra*).

184. Example 2. Each transceiver supports a total of 60,000 octets of shared interleaver/deinterleaver memory. If the service provider desires to provide a VDSL2 service that requires 30,000 octets of memory in each transceiver for the downstream service and 30,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 30,000 octets in each transceiver are used for the downstream path and 30,000 octets are used for the upstream path as illustrated below.



185. On the other hand, if the service provider desires to provide a VDSL2 service that requires 40,000 octets of memory in each transceiver for the downstream service and 20,000 octets of memory in each transceiver for the upstream service, the 60,000 octets of memory in each transceiver could be allocated between the interleaver and deinterleaver functions such that 40,000 octets in each transceiver are used for the downstream path and 20,000 octets are used for the upstream path as illustrated below.



186. Therefore, unlike LB-031 where 10,000 octets of memory are unused and the service provider could not provide the service to the customer, when shared memory, which can be allocated between the interleaver function or deinterleaver function, is used, memory that would otherwise go unused can be allocated to one

function or the other depending on messages that are, in part, dependent on the service requirements. As illustrated by these examples, the VTU-R is capable of allocating 10,000 octets of its memory to the upstream interleaving function at one time but allocating the same 10,000 octets of its memory to the downstream deinterleaving function at another time. This provides flexibility that enables the transceivers to meet different service requirements.

187. The claimed allocation of memory requires allocating the memory between an interleaving function and a deinterlacing function according to a message. LB-031 does not teach this claim element. Instead, as illustrated above, it allows a transceiver to determine how much of its pre-allocated downstream memory (i.e., interleaver memory in the VTU-O and deinterleaver memory in the VTU-R) and how much of its pre-allocated upstream memory (i.e., deinterleaver memory in the VTU-O and interleaver memory in the VTU-R) can be used.

188. It is therefore my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 19 of the '473 Patent.

b. LB-031 does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

189. LB-031 does not disclose, teach, or suggest these claim elements. As discussed in the Overview of LB-031 Section, and in the section immediately above, as well as in connection with claim 1 of the '048 patent, *supra*, LB-031 does not disclose any sharing of memory within a transceiver. *See* § VI.A.1; *see also* §§ VI.A.2.a, VI.A.5.a.

Therefore, in a transceiver operating in accordance with LB-031, no portion of memory may be allocated to an interleaving function at one time or a deinterleaver function at another time depending on a message.

190. As discussed in paragraphs 177-182 above with respect to the Example 1, according to the teachings of LB-031, the dedicated interleaver memory may not at any particular time be allocated to the deinterleaver function and the dedicated deinterleaver memory cannot at any particular time be used for the interleaver function. The exchange of capabilities in LB-031, even assuming it is accomplished through messages exchanged during initialization, would not allow any portion of memory to be allocated to an interleaver function at one time or a deinterleaver function at another time depending on a message. Rather, any messages contemplated by LB-031 are used only to select the smaller of the transmitter or receiver capabilities. This may result in portions of memory that are unused, as explained in paragraphs 136-139. It will not result in a portion of memory being used for one function or the other at a particular time depending on a message, as claimed.

191. Confusingly, Dr. Jacobsen argues that because a transceiver can transmit and receive at the same time, this element is met. *See* Jacobsen Report at ¶ 246. She does not explain how transmitting and receiving at the same time has anything to do with this claim element. In fact, the conclusion she draws from this is that LB-031 discloses that the shared memory allocated to the interleaver is used at the same time as the shared memory allocated to the deinterleaver. *Id.* The conclusion has no bearing on whether, and does not prove that, LB-031 discloses "at least a portion of the memory

may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

192. For the foregoing reasons, it is my opinion that LB-031 fails to disclose all elements of claim 19 of the '473 patent and therefore fails to render claim 19 of the '473 patent obvious.

B. The Asserted Claims Are Not Obvious Over the Combination of LB-031 and Mazzoni

193. It is my opinion and conclusion that Mazzoni alone or in combination with LB-031 fails to disclose or suggest each element of the Asserted Claims, and hence fails to render the Asserted Claims obvious as described in detail, below.

194. It is also my opinion that regardless of the disclosure of LB-031 and Mazzoni individually, a person of ordinary skill in the art would not be motivated to combine the teachings of LB-031 with the teachings of Mazzoni at least for the reasons described in Section VI.B.2, *infra*.

195. An overview of LB-031s has been provided in Section VI.A.1, *supra.*

1. Overview of Mazzoni

196. The disclosure of Mazzoni is based on the premise that there is a finite group of data rate pairs, where each data rate pair comprise a predetermined upstream data rate and a predetermined downstream data rate). *See* Mazzoni at 1:65 – 2:2 ("The invention therefore provides a device for sending/receiving digital data that is capable of processing different bit rates from a group of predetermined bit rates (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system)."),

3:62 – 4:14 (describing six symmetrical and six asymmetrical data rate pairs). Mazzoni also refers to these data rate pairs as services, where a service utilizes one predetermined data rate in the upstream direction and another predetermined data rate in the downstream direction. *See id*. In a symmetric service, the upstream data rate is the same as the downstream data rate. *Id*. at 3:62 – 4:2. In an asymmetric service the two are different. *Id*. at 4:3-14. Mazzoni describes higher and lower bit rate examples of six possible symmetrical services:

> The VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6. That is, the information bit rates in the two transmission directions (i.e., from the operator to the user and from the user to the operator) are exactly the same. The service S1 with the lowest bit rate has a bit rate of 32x64 kbit/s, for example, and the fastest symmetrical service S6 has a bit rate of 362x64 kbit/s.

Id. at 3:62 – 4:2. Mazzoni also describes example asymmetrical services with higher bit rates for the downstream direction:

> With the VDSL system, the operator can also provide asymmetrical services A1-A6. These are services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction). The first asymmetrical service A1 has a bit rate in the uplink direction of 32x64 kbit/s, for example, and a bit rate in the downlink direction of 100x64 kbit/s. The asymmetrical service having the highest global information bit rate (uplink bit rate+downlink bit rate) is the service A6. The bit rate of the service A6 in the uplink direction is equal to 32x64 kbit/s and in the downlink direction is equal to 832x64 kbit/s.

Id. at 4:3-14.

197. Mazzoni describes the assignment of interleaver memory and deinterleaver memory for each of the predefined data rate pairs (services). To

accomplish this, Mazzoni proposes using predefined I and M parameter values for its interleaving means, and predefined I′ and M′ parameter values for deinterleaving means for each data rate pair (i.e., service).

198. This fixed correspondence of a data rate pair to predefined I and M parameter values (for interleaving) and predefined I′ and M′ parameter values (for deinterleaving) is explained by Mazzoni as follows:

> These parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means. This is done according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I′ and M′).

Id. at 5:24-30.

199. "TO" in the above quoted language refers to a device at the "operator end." *Id.* at 4:3:59-60. "TU" refers to a device at the "user end." *Id.* Because the TO interleaves information to be transmitted downstream and deinterleaves information it receives in the upstream direction, the I and M interleaving parameters are associated with information sent by the TO, and similarly the I′ and M′ parameters are associated with information received by the TO. *See, e.g.,* Mazzoni at 5:27-30; Jacobsen Report at ¶¶ 96-100 (describing how the terms "interleaving" and "deinterleaving" are used in connection with the terms "upstream" and "downstream" communications in ADSL and VDSL).

200. Mazzoni explains that the predefined values of I and M specify the amount of predefined memory for the downstream interleaver of TO (and hence the downstream deinterleaver of TU) , and I′ and M′ specify the amount of predefined

memory for an upstream deinterleaver of TO (and hence the downstream interleaver of TU), for a particular data rate pair (i.e., service). *See* Mazzoni at 6:38-43 ("More particularly, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to Ix(I-l)xM/2. Similarly, the size of the second memory space ESM2 required to support the uplink bit rate is equal to I'x(I'-1)xM'/2."); *see also id*. at 6:53-59 ("A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD may retrieve the corresponding values of I, M, I' and M' from the stored table."); *id*. at 5:24-30. These values are stored in a table within the modem and retrieved at the time of modem installation. *See* Mazzoni at 5:22-23, 6:51-55. Specifically, Mazzoni explains:

> The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. **A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage.** When the modem is installed at the end of the line, and depending on the service actually provided by the operator, **the control means MCD may retrieve the corresponding values of I, M, l' and M' from the stored table**. These values are delivered to the addressing means MADl and MAD2, the structure of which is described in more detail with reference to FIGS. 7 and 8.

Mazzoni at 6:51-61 (emphasis added).

201. As shown above in the quoted disclosure, the I, M, I', and M' parameter values are all predetermined for each data rate pair from a group of predefined data rate pairs and are stored in table. Mazzoni explains that at the time of the installation of the modem, the modem's memory is configured according to the I, M, I', and M' values

retrieved from a table. Which values are retrieved depends on "the service actually provided by the operator," i.e., on the upstream and the downstream data rate pair configuration that is being provided by the service provided for the modem.

202. Dr. Jacobsen's description of Mazzoni is incomplete, and thus does not accurately characterize Mazzoni's teachings, because it overlooks Mazzoni's fundamental premise that a predefined data rate pair service and corresponding predefined I, M, I′ and M′ values will be fixed at the time of installation of a modem. For example, Dr. Jacobsen, citing Mazzoni at 6:19-50, states that the I, M, I′, and M′ parameters "can be determined from maximum and minimum memory size capacities that are easily calculable using downlink and uplink bit rates the number of bits affected by noise, and RS error correction." *See* Jacobsen Report at ¶ 256. Dr. Jacobsen does not explain further what this "determination" is, or when it occurs. *See id*. Yet, the portion of Mazzoni that she cites simply describes examples of how one can choose the predetermined values of the I, M, I′, and M′ parameters that are then stored in a table for retrieval at the time of installation of the modem. *See* Mazzoni at 6:19-50.

203. Also, because the data rate pair options are predetermined (and hence known in advance), and because there is a predetermined set of values for the I, M, I′ and M′ parameters for each predetermined data rate pair, there is no need for a device in Mazzoni to obtain any additional information from a device at the other end of the communication line in order to implement the memory assignment described by Mazzoni. Such an assignment is carried out in a sole reliance on the predetermined set

of I, M, I′, and M′ parameters stored in a table and retrieved by the control means at the time of installation of the deice. *See* Mazzoni at 6:53-59.

2. A Person of Ordinary Skill in the Art Would Not Combine the Teachings of LB-031 with the Teachings of Mazzoni

204. A person of ordinary skill in the art at the time of the invention of the Family 3 Patents would not look to the teachings of Mazzoni when implementing the teachings of LB-031, or *vice versa*. In fact, as explained below, the two references are so different than a person of ordinary skill in the art would be discouraged from looking to the teaching of the other reference.

205. An overview of LB-031 has been provided in Section VI.A.1, *supra*. The overview of Mazzoni has been provided in Section VI.B.1, *supra*.

206. Dr. Jacobsen asserts that "both Mazzoni and LB-031 disclose VDSL transceivers." *See* Jacobsen Report at ¶ 346. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.B.7 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the VDSL standard was still under development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for VDSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni and

LB-031 are purportedly both directed to different proposals for yet-to-be-defined VDSL transceivers, would not have made their combination obvious.

207. Dr. Jacobsen then states that "both Mazzoni and LB-031 are concerned with limiting the size of memory used for interleaving and deinterleaving." *See* Jacobsen Report at ¶ 347. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.B.7 of the Jacobsen Report, is again not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references.

208. Also, this generalization is inaccurate. As explained in VI.A.1, *supra*, LB-031 is concerned with providing a solution that meets certain delay requirements specified in units of time, while allowing use of larger dedicated interleaver or deinterleaver memories if both transceivers support more than the minimum required by a standard. There is no technique described in LB-031 for "limiting the size of memory used for interleaving and deinterleaving," contrary to Dr. Jacobsen assertions. *See* § VI.A.1. Rather, as I explained above, LB-031 actually wastes memory by leaving portions of memory unused where one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating. *See* § VI.A.1 and ¶¶ 176-187, *supra*. Because LB-031 wastes memory, a POSITA would be motivated **not** to use the teachings of LB-031 if they were concerned with reducing memory requirements.

209. Dr. Jacobsen states that: "[a] skilled artisan wishing to implement the VDSL transceiver of Mazzoni would have been motivated to include the initialization

message of LB-031 so that the VTU-O and VTU-R of Mazzoni could choose values for the parameters I, M, I′ and M′ that would not exceed the size of the shared memory at the selected downstream and upstream bit rates." *See* Jacobsen Report at ¶ 350. This is incorrect.

210. A POSITA would not look to add a message (from LB-031 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I', and M' parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. *See* Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the maximum supported interleaver or deinterleaver memory size (assuming such a message is even disclosed per LB-031) because all data rate pairs and their corresponding I, M, I', and M' values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant and serve no useful purpose.

211. An additional reason why LB-031's exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible. Take an example where we assume that, per LB-031, the VTU-R (i.e., TR of Mazzoni) transmits to the VTU-O (i.e., TU of Mazzoni) a message that specifies the maximum downstream deinterleaver memory size that it supports and the maximum

upstream interleaver memory size that it supports. Using the predefined services described in Mazzoni, i.e., S1-S6 and A1-A6 (*see* Mazzoni at 3:62 – 4:14), the maximum downstream deinterleaver memory that Mazzoni is capable of supporting is determined by reference to the A6 service and the maximum upstream interleaver memory that Mazzoni is capable of supporting is determined by reference to the S6 service. The A6 service provides a downstream bit rate of 832x64 kbit/s and requires 24,960 bytes of deinterleaver memory. *See id.* at 6:11-30 (describing calculation of required deinterleaver memory size). The S6 service provides an upstream bit rate of 362x64 kbit/s. Per the calculations described at 6:11-30 of Mazzoni, the S6 service requires that the VTU-R be capable of supporting a maximum upstream interleaver memory of 10,860 bytes. If the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum downstream deinterleaver memory of 24,960 bytes and a maximum upstream interleaver memory of 10,860 bytes, this information would be useless to the VTU-O. First, it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation. Second, neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes (as determined by the combined upstream and downstream bit rates of the A6 service). *See id.* at 4:18-22 and 6:45-50.

212. While Dr. Jacobsen's asserted motivations to combine LB-031 and Mazzoni fail to account for the fact that Mazzoni's transceivers are preconfigured at the

time of installation with all the information they need, in another section (specifically in Section IX.G.5 of the Jacobsen Report) she admits that "Mazzoni further discloses keeping a table of values of the interleaver parameters, indexed by service identifies, in the transceiver." *See* Jacobsen Report at ¶ 626 (citing Mazzoni at 6:51-61).

213. A POSITA at the time of the Family 3 Patent inventions would not combine the teachings of Mazzoni with the teachings of LB-031. If fact, a POSITA would be discouraged from doing so. Because Mazzoni teaches that an assignment of the memory is performed at the time of the installation of the modem based on a table, and not a message, adding a message to this system per LB-031 would be unnecessary, redundant, and create useless complexity during initialization. Further, because Mazzoni is concerned with supporting a finite set of predefined service configurations (i.e., data rate pairs and corresponding interleaver/deinterleaver parameter values).

214. For at least the foregoing reasons, Dr. Jacobsen has not demonstrated that a POSITA would have been motived to combine LB-031 with Mazzoni in the manner she proposes.

3. The Combination of LB-031 and Mazzoni Does Not Render Claim 1 of the '048 Patent Obvious

215. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.3 below, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 1 of the '048

patent, and hence fails to render claim 1 of the '048 patent obvious as described in detail, below.

a. The combination of LB-031 and Mazzoni does not disclose a system that allocates shared memory.

216. As explained in Section VI.A.2.a, *supra*, LB-031 does not disclose a system that allocates shared memory. LB-031 also does not disclose the exchange of information that would be useful for allocating shared memory. As explain above, LB-031 only describes exchanging information about the maximum size of dedicated interleaver memory and, separately, the maximum size of dedicated deinterleaver memory supported by a transceiver. At least for the reasons explained, in paragraph 211 above, this information could not be used by a Mazzoni transceiver to allocate shared memory.

217. As explained above in the Overview of Mazzoni section, Mazzoni relies on a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values, I, M, I' and M'. *See* § VI.B.1. The predetermined assignment takes place when the modem is installed by retrieving the bit rates and parameter values from a stored table. Mazzoni at 6:55-69. Thus, contrary to Dr. Jacobsen's opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. *See also*, § VI.B.3.d, *infra*.

218. Mazzoni does not disclose the claimed system for allocating shared memory at least because Mazzoni does not disclose a transceiver that (1) transmits or receives a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver (*see* § VI.B.3.b, *infra*); (2) determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory (*see* § VI.B.3.c, *infra*); and (3) allocating a first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message (*see* § VI.B.3.d, *infra*).

219. Also, because a POSITA would have no rational reason to combine the LB-031 with Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 1 of the '048 patent obvious.

b. The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver.

220. Contrary to Dr. Jacobsen's assertion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that the bit rate information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, as is described in LB-031. Jacobsen Report

at ¶ 269. The "information" she is referring to is the parameters I, M, I′ and M′. But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I, M, I′ and M′. *See id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I, M, I′ and M′ are not exchanged in any message; rather, as discussed above in Section VI.B.1, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

221. One of the passages Dr. Jacobsen cites for this assertion, Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I′ and M′ parameters are exchanged in messages. Rather, this passage simply describes the use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this elsewhere in her report. *See, e.g.,* Jacobsen Report at ¶ 595 ("Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all

of the services would have to be identified ahead of time and stored in the transceivers."); *see also id.* at ¶ 626.

222. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to "the bit rate actually processed by the send/receive device (modem)" is referring to one of the predetermined bit rates for a predetermined service. Mazonni at 1:65 – 2:2 ("The invention therefore provides a device for sending/receiving digital data that is capable of ***processing different bit rates from a group of predetermined bit rates*** (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).").

223. Because Mazzoni does not describe any message specifying an amount of memory that can be allocated to an interleaver or to a deinterleaver, and because LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni (*see* § VI.B.2, *supra*), the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of transmitting or receiving a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to an interleaver" and, at least for this reason, claim 1 of the '048 patent is not obvious in view of LB-031 and Mazzoni.

c. The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory.

224. Dr. Jacobsen assert that Mazzoni discloses this limitation. I disagree. While Mazzoni describes the math calculations by which the interleaver and deinterleaver memory sizes can be determined from the upstream and downstream bit rates and the parameters I, M, I′ and M′ (*see* Mazzoni at 6:11-50), there is no disclosure in Mazzoni that these memory sizes or parameters are determined by Mazzoni's transceiver. Rather, these values are predetermined, stored in a table, and retrieved for use at the time of installation of the transceiver. *Id.* at 6:53-59 ("A table of values for the parameters I, M, I′ and M′ can therefore be stored in the coding/decoding stage. When the modem is installed . . . , the control means MCD may retrieve the corresponding values of I, M, I′ and M′ from the stored table."). Because these values are stored prior to installation, they may be calculated by hand or by separate computer before loading into a stored table on the transceiver.

225. Simplification is a major benefit of Mazzoni's scheme of providing devices that are preconfigured to provide one of 12 service profiles with predetermined data rates and predetermined interleaver and deinterleaver parameters. Requiring Mazzoni's transceiver to calculate interleaver parameters or memory sizes each time it is going to use these values would be contrary to the goal of simplification, particularly where only a limited number of service profiles are needed and where all necessary information is stored prior to installation.

226. Because Mazzoni does not describe a transceiver that determines interleaver parameters or memory sizes, and because requiring Mazzoni to do so it would be contrary to Mazzoni's simplified scheme of storing predetermined values, the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of determining an amount of memory required by the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes within the shared memory" and, at least for this reason, claim 1 of the '048 patent is not obvious in view of LB-031 and Mazzoni.

227. Also, because a POSITA would be discouraged from combining the teaching of LB-031 with the teachings of Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 1 of the '048 patent obvious.

d. The combination of LB-031 and Mazzoni does not disclose a transceiver that is capable of allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message.

228. As explained in Section VI.A.2.c, *supra*, LB-031 does not disclose or suggest allocating the first number of bytes of the shared memory to the interleaver to interleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message. This is so at least because LB-031 does not disclose shared memory, as explained in Sections VI.A.2.a, VI.A.5.a.ii.

229. As explained in Section VI.B.3.b, *supra*, Mazzoni does not disclose transmitting or receiving any message with interleaver or deinterleaver parameters. Further, as explained in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose "a transceiver that is capable of allocating a first number of bytes of the shared memory to the interleaver to interleave the first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message" and, at least for this reason, claim 1 of the '048 patent is not obvious in view of LB-031 and Mazzoni.

230. I note that Dr. Jacobsen cites to Mazzoni at column 1:19-27 for purportedly disclosing the portion of this claim element that recites "wherein the allocated memory for the interleaver does not exceed the maximum number of bytes in the message." Jacobsen Report at ¶ 280. She does not provide any explanation for how this portion of Mazzoni discloses this claim element. I have reviewed this portion of Mazzoni and it does not in any way disclose this claim element. Rather, it is a generic background section regarding VDSL, asymmetrical and symmetrical data rates, and the fact that modems that operate at predetermined bit rates have interleaver and deinterleaver

memories that depend on that bit rate. This background section actually emphasizes, consistent with my opinions, that Mazzoni is directed to providing predefined services with predetermined bit rates and corresponding predefined interleaver and deinterleaver parameters, which would not require, or benefit from, an exchange of capabilities per LB-031.

4. The Combination of LB-031 and Mazzoni Does Not Render Claim 5 of the '381 Patent Obvious

231. It is my opinion for the reasons provided in Section VI.B.2above and as further discussed in this Section VI.B.4, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 5 of the '381 patent, and hence fails to render claim 5 of the '381 patent obvious as described in detail, below.

a. The combination of LB-031 and Mazzoni does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver.

232. As explained in Section VI.A.3.a, *supra*, LB-031 does not disclose a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver. *See also* § VI.A.2.a, *supra*; *see generally* § VI.A.1, *supra*.

233. More generally, LB-031 also does not disclose the exchange of information that would be useful for allocating shared memory. *See id*. As explained above, LB-031

only describes exchanging information about the maximum size of dedicated interleaver memory and, separately, the maximum size of dedicated deinterleaver memory supported by a transceiver. At least for the reasons explained, in paragraph 211 above, this information could not be used by a Mazzoni transceiver to allocate shared memory. As described in Section VI.A.2.a, LB-031 does not include any disclosure directed to allocating shared memory in a transceiver. Consequently, at least for the same reasons as described with respect to claim 1 of the '048 patent, LB-031 fails to disclose this element of claim 5 of the '381 patent.

234. As explained above in the Overview of Mazzoni section, Mazzoni relies on a predetermined assignment of a service that has a predetermined pair of upstream and downstream bit rates and a corresponding set of predetermined interleaver and deinterleaver parameter values, I, M, I' and M'. *See* § VI.B.1. The predetermined assignment takes place when the modem is installed by retrieving the bit rates and parameter values from a stored table. Mazzoni at 6:55-69. Thus, contrary to Dr. Jacobsen's opinion with respect to claim 1 of the '048 patent (incorporated by reference here), Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters as described above in connection with claim 1 of the '048 patent. *See also*, § VI.B.3.d, *supra*.

235. Furthermore, Dr. Jacobsen did not identify any portions of LB-031 that disclose a non-transitory computer-readable information storage media having stored thereon instruction that are executed by a processor in Section IX.B.4.a of the Jacobsen Report addressing this claimed element. Nor has she done that in Section IX.A.4.a of

the Jacobsen Report, which seems relevant but was not even incorporated by reference. *See* Jacobsen Report at ¶ 210; *see also id*. at ¶ 300. With respect to LB-031, as explained in Section VI.A.3.a above, Dr. Jacobsen without any support simply draws an inference that "[o]ne of ordinary skill in the art would have understood that a source code and instructions for such transceivers could be stored on computer-readable information storage media, and could be executed by a processor." *See id*. Dr. Jacobsen makes the same argument with respect to Mazzoni. *See* Jacobsen Report at ¶ 300 ("One of ordinary skill in the art would have understood that source code and instructions for such transceiver could be stored on computer-readable information storage media, and could be executed by a processor, for example, as source or object code.").

236. As explained in Section VI.A.3.a, *supra*, Dr. Jacobsen's conclusion is wrong on its face. Source code (or object code) cannot be executed by a processor. A POSITA would understand that source code (or object code) is a term of art referring to uncompiled and non-executable human readable code.

237. Also, as explained in Section VI.A.3.a, *supra* with respect to LB-031, and now with respect to Mazzoni, even ignoring the fact that Dr. Jacobsen's conclusion is wrong on its face, Dr. Jacobsen did not show that any element of claim 5 of the '381 patent is performed by executing instructions stored on a non-transitory computer-readable information media. A POSITA would understand that it is possible that one or more of the claimed functions could be implemented in hardware, and therefore would not necessarily have to be carried out through an execution of instructions stored on a non-transitory computer-readable media. Dr. Jacobsen did not even attempt to show

one way or another with which of these possibilities LB-031 or Mazzoni would be concerned with respect to each claimed function.

238. Finally, Mazzoni does not disclose the claimed non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver at least because Mazzoni does not disclose (1) transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver (*see* § VI.B.4.b, *infra* and § VI.B.3.b, *supra*); (2) determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory (*see* § VI.B.4.c, *infra* and § VI.B.3.c, *supra*); and (3) allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message (*see* § VI.B.4.d, *infra* and § VI.B.3.d, *supra*).

239. Also, because a POSITA would have no rational reason to combine the LB-031 with Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 5 of the '381 patent obvious.

240. It is my opinion that LB-031 does not disclose, teach, or suggest this claim element of claim 5 of the '381 patent and therefore fails to render claim 5 of the '381 Patent obvious.

b. The combination of LB-031 and Mazzoni does not disclose transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver.

241. Contrary to Dr. Jacobsen's assertion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters. Dr. Jacobsen asserts that her discussion with respect to an interleaver in Section IX.B.3.c is equally applicable to a deinterleaver. *See* Jacobsen Report at ¶ 303. I have addressed the arguments from that section in Section VI.B.3.b, *supra*.

242. Because Mazzoni does not describe any message specifying an amount of memory that can be allocated to an interleaver or to a deinterleaver, and because LB-031's exchange of interleaver and deinterleaver capabilities would be useless and incompatible with Mazzoni (*see* § VI.B.2, *supra*), the combination of LB-031 and Mazzoni does not disclose "transmitting or receiving, by the transceiver, a message during initialization specifying a maximum number of bytes of memory that are available to be allocated to a deinterleaver" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

c. The combination of LB-031 and Mazzoni does not disclose determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory.

243. Dr. Jacobsen assert that Mazzoni discloses this limitation by incorporating her arguments from paragraph 269 of the Jacobsen Report. *See* Jacobsen Report at ¶

305. I disagree for the reasons discussed in Section VI.B.3.c. My arguments directed to interleaving are equally applicable to deinterleaving.

244. Because Mazzoni does not describe a transceiver that determines deinterleaver parameters or memory sizes, and because requiring Mazzoni to do so it would be contrary to Mazzoni's simplified scheme of storing predetermined values, the combination of LB-031 and Mazzoni does not disclose "determining, at the transceiver, an amount of memory required by the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes within a shared memory" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

245. Also, because a POSITA would be discouraged from combining the teaching of LB-031 with the teachings of Mazzoni, as explained in Section VI.B.2, *supra*, the combination of the combination of LB-031 and Mazzoni does not render claim 5 of the '381 patent obvious.

d. The combination of LB-031 and Mazzoni does not disclose allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message.

246. As explained in Sections VI.A.3.c and VI.A.3.d, LB-031 does not disclose allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message. This is so at

least because LB-031 does not disclose shared memory, as explained in Sections VI.A.2.a, VI.A.5.a.ii.

247. As explained in Section VI.B.3.b, *supra*, Mazzoni does not disclose transmitting or receiving any message with interleaver or deinterleaver parameters. Further, as explained in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose "allocating, in the transceiver, a first number of bytes if the shared memory to the deinterleaver to deinterleave a first plurality of Reed Solomon (RS) coded data bytes for transmission at a first data rate, wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message" and, at least for this reason, claim 5 of the '381 patent is not obvious in view of LB-031 and Mazzoni.

248. I also note that in a section incorporated by reference, Dr. Jacobsen cites to Mazzoni at column 1:19-27 for purportedly disclosing the portion of the claim element that recites "wherein the allocated memory for the ***interleaver*** does not exceed the maximum number of bytes in the message." Jacobsen Report at ¶ 280. She does not provide any explanation for how this portion of Mazzoni discloses this claim element. I have reviewed this portion of Mazzoni and it does not in any way disclose this claim

element. Rather, it is a generic background section regarding VDSL, asymmetrical and symmetrical data rates, and the fact that modems that operate at predetermined bit rates have interleaver and deinterleaver memories that depend on that bit rate. This background section actually emphasizes, consistent with my opinions, that Mazzoni is directed to providing predefined services with predetermined bit rates and corresponding predefined interleaver and deinterleaver parameters, which would not require, or benefit from, an exchange of capabilities per LB-031. At least for the same reason, Mazzoni does not disclose this claim element that recites "wherein the allocated memory for the ***deinterleaver*** does not exceed the maximum number of bytes specified in the message."

5. The Combination of LB-031 and Mazzoni Does Not Render Claim 13 of the '882 Patent Obvious

249. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.5, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 13 of the '882 patent, and hence fails to render claim 13 of the '882 patent obvious as described in detail, below.

a. The Combination of LB-031 and Mazzoni does not disclose a system that allocates shared memory.

250. LB-031 does not disclose, teach, or suggest this claim element of claim 13 of the ’882 Patent for the same reason as discussed with respect to the same claim element of claim 1 of the ‘048 Patent. *See* § VI.B.3.a.

b. The Combination of LB-031 and Mazzoni does not disclose other elements of this claim.

251. Dr. Jacobsen adopts wholesale her arguments with respect to claim 5 of the of the ‘381 patent (elements 5[b] – 5[h]) as her argument with respect to claim 13 of the ‘882 patent (elements 13[c] through 13[i], respectively). *See* Jacobsen Report at ¶ 320.

252. Accordingly, I hereby incorporate my arguments with respect to claim elements of claim 5 of the ‘381 patent, and also claim 1 of the ‘048 Patent as rebuttal augment for the respective claim elements of claim 13 of the ‘882 patent.

253. Specifically, using the claim element numbering from Dr. Jacobsen Report (*see* Appendix C to Jacobsen Report), I hereby incorporate herein the following sections of this report:

- with respect to elements 13[b] and 13[c], I incorporate §§ VI.B.3.b, VI.B.4.b, *supra*;
- with respect to elements 13[b] and 13[d], I incorporate §§ VI.B.3.c, VI.B.4.c, *supra*;
- with respect to elements 13[b], 13[e], and 13[f], I incorporate §§ VI.B.3.d, VI.B.4.d, *supra*;

254. The Combination of LB-031 and Mazzoni does not disclose, teach, or suggest the above claim elements of claim 13 of the '882 Patent for the same reason as discussed with respect to the substantially similar claim elements of claim 5 of the '381 Patent, and claim 1 of the '048 Patent. At least for these reasons, it is my opinion and conclusion that the Combination of LB-031 and Mazzoni fail to disclose or suggest all elements of claim 13 of the '882 Patent.

6. The Combination of LB-031 and Mazzoni Does Not Render Claim 19 of the '473 Patent Obvious

255. It is my opinion for the reasons provided in Section VI.B.2 above and as further discussed in this Section VI.B.6, that a POSITA would not combine LB-031 and Mazzoni or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that LB-031 in combination with Mazzoni fails to disclose each element of claim 19 of the '473 patent, and hence fails to render claim 19 of the '473 patent obvious as described in detail, below.

a. The Combination of LB-031 and Mazzoni does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.

256. For the reasons discussed above in Section VI.A.5.a, LB-031 does not disclose this claim element.

257. Further, contrary to Dr. Jacobsen's opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or

deinterleaver memory allocations could be based). Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message." Jacobsen Report at ¶ 339. The "information" she is referring to is the parameters I, M, I′ and M′. But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I, M, I′ and M′. *See id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I, M, I′ and M′ are not exchanged in any message; rather, as discussed above in Section VI.B.1, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

258. One of the passages Dr. Jacobsen cites for this assertion, Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I′ and M′ parameters are exchanged in messages. Rather, this passage simply describes the

use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this elsewhere in her report. *See, e.g.*, Jacobsen Report at ¶ 595 ("Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers."); *see also id.* at ¶ 626.

259. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to "the bit rate actually processed by the send/receive device (modem)" is referring to one of the predetermined bit rates for a predetermined service. Mazzoni at 1:65 – 2:2 ("The invention therefore provides a device for sending/receiving digital data that is capable of ***processing different bit rates from a group of predetermined bit rates*** (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system).").

260. While neither LB-031 or Mazzoni individually disclose this claim element, as explained in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to Mazzoni's stored predefined service data rates and

interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported interleaver and deinterleaver sizes per LB-031 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size. Accordingly, the combination of LB-031 and Mazzoni does not disclose "a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver" and, at least for this reason, claim 19 of the '473 patent is not obvious in view of LB-031 and Mazzoni.

b. The combination of LB-031 and Mazzoni does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

261. For the reasons discussed above in Section VI.A.5.b, LB-031 does not disclose this claim element.

262. With respect to Mazzoni, Dr. Jacobsen's conclusion in paragraph 343 of the Jacobsen Report that "[o]ne of ordinary skill in the art would have understood that the interleaving means and the deinterleaving means would operate at the same time" does not appear to address this claim element. That an interleaver and deinterleaver operate at the same time does not disclose or require that a portion of the memory be allocated to the interleaver function or deinterleaver function at any one particular time depending on the message. Perhaps this was a cut and paste error and was intended for the element of claim 5 of the '381 patent, which recites: "wherein the shared memory

allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver."

263. Dr. Jacobsen further asserts paragraph 344 of the Jacobsen Report that "Mazzoni also discloses that the portion of the memory allocated to the interleaving function or the deinterleaving function at any one particular time is dependent on the message." I disagree. As I explained in the section immediately above, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Further, as I explained in the section immediately above and in Section VI.B.2, *supra*, LB-031's exchange of interleaver and deinterleaver capabilities is redundant to and incompatible with Mazzoni.

264. For at least the foregoing reasons, the combination of LB-031 and Mazzoni does not disclose "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message" and, at least for this reason, claim 19 of the '473 patent is not obvious in view of LB-031 and Mazzoni.

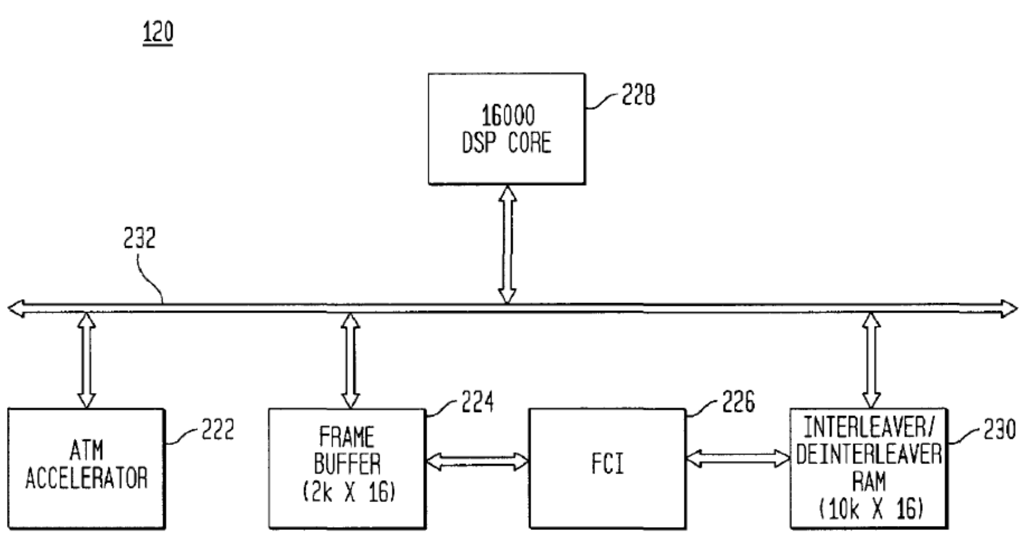
C. The Asserted Claims Are Not Obvious Over Fadavi-Ardekani in Combination with ITU-T Recommendation G.993.1

1. Overview of Fadavi-Ardekani

265. As an initial matter, U.S. Patent No. 6,707,822 to Fadavi-Ardekani et al., hereinafter Fadavi, was considered by the USPTO during the prosecution of the parent, U.S. Patent 7,831,890, and the claims were allowed over Fadavi. *See*, Notice of

Allowance for ’890 patent. Fadavi is also cited on the face of each of the Family 3 Patents.

266. Fadavi discloses “an Asymmetric Digital Subscriber Line (ADSL) transceiver that manages multiple asynchronous ADSL sessions, synchronizing the digital signal processing tasks for the sessions with a buffering and scheduling scheme such that the various transceiver components operate seamlessly (i.e., in a semi-synchronous fashion).” Fadavi at 2:62-68. Fadavi defines an agent as “a transceiver component for performing some function.” *Id.* at 5:62-63. Fadavi discloses several agents including the ATM accelerator, the Framer/Coder/Interleaver (FCI) and the DSP core. Set forth below is a block diagram of the transceiver taught by Fadavi.



Fadavi at FIG. 2.

267. The organization of the various agents and related components of Fadavi's transceiver is as follows:

> An Asynchronous Transfer Mode (ATM) Accelerator provides the network interface to multiple ATM channels for multiple asynchronous ADSL sessions. The ATM accelerator transfers frame data to a Frame Buffer (FB) as controlled by a Digital Signal Processing (DSP) core. The FB provides a dual access memory that is used in a **ping-pang** fashion, based on the logic level of the virtual clock, for the communication of data between the ATM accelerator and a Framer/Coder/Interleaver (FCI). The FCI performs various processing tasks on the frame data and also interfaces the DSP core through an Interleave/De-interleave Memory (IDIM), which holds DMT frames of data and may also be utilized in a ping-pang fashion. . . . The DSP core controls operation of the ATM accelerator and the FCI and performs various processing tasks such as moving data to/from the FB and the IDIM.

Fadavi at 3:8-25 (emphasis added).

> "Ping-pang" means that areas of the memory buffer are alternately utilized exclusively by one agent (a transceiver component for performing some function) and then by a second agent. As one area of memory is being used by a first agent, another area of memory can be used by a different agent.

Id. at 5:60-65.

> The ATM accelerator provides those functions that are responsible for data transport for a plurality of data streams communicated via twisted pair media. The data may be transported on anyone of a plurality of programmable bearer channels. The data is synchronized into an appropriate one of the plurality of programmable bearer channels and the channels multiplexed in the ATM accelerator as determined by the ADSL standard. The ATM accelerator subjects this framed data to various operations that calculate a plurality of complex numbers representing DMT tones. The ATM accelerator subsequently transfers this DMT tone data on the twisted-pair media.

Id. at 5:43-54.

> The FCI . . . performs various tasks on payload data including: framing/de-framing, cyclic redundancy check generation/checking (CRCing), scrambling/descrambling, Reed-Solomon encoding/decoding, and interleaving/de-interleaving. . . . All functionalities of the FCI are

> provided as per ADSL standards. In a preferred embodiment of the invention, approximately four G.lite (ITU G.992.2) or approximately four ADSL (ANSI Tl.413-1998) sessions are supported by the FCI.

Id. at 6:20-23.

268. Fadavi explains that the FB and IDIM memories are accessed in ping-pang fashion by the agents. Specifically, [t]he Frame Buffer (FB) 224 provides a dual access memory that is used in a ping-pang fashion to transfer unframed bearer channel data between the ATM accelerator 222 and the FCI 226." *Id.* at 5:57-60. The FCI and ATM accelerator first perform reading processes and then loading processes, reading RX data first before loading the TX data into the FB.

269. The IDIM is used in a ping-pang fashion by the FCI and DSP core. Specifically,

> The Interleave/De-Interleave Memory (IDIM) 230 provides a memory through which the FCI 226 interfaces the DSP core 228. The IDIM holds DMT frames of data and may be utilized in a ping-pang fashion. The IDIM is used to transfer framed, coded and possibly interleaved data frames between the FCI core and the DSP Core.

Id. at 6:55-60.

> In a preferred embodiment of the invention, the IDIM is allocated as 10 Kx16 (i.e., 20 K) Random Access Memory (RAM), which supports approximately four G .lite or approximately four standard ADSL session/s at less than full interleave depth. The size of the IDIM and the interleave depth may be varied so that a different number of sessions may be supported by the transceiver of the invention. The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes

> per session for upstream processing, for a total of 72 Kbytes for four sessions. A fast path buffer is also required for fast path data in both the interleave and dc-interleave processes and requires 256 bytes of RAM per session, or a total of 1 Kbytes for four sessions. Since the smallest RAM block currently available is 1 Kx16, 1 Kx160 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path). An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path). With a lesser interleave depth, additional sessions may be supported with the same size buffer. With a larger buffer, additional session may be supported.

The IDIM is used in a ping-pang fashion by the FCI and DSP core.

270. Based on the foregoing, Fadavi teaches using an IDIM whose size is "derived by multiplying the maximum codeword length by the maximum interleaver depth." To support additional sessions, Fadavi teaches reducing the interleaver depth or using a larger memory.

2. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 1 of the '048 patent

a. Fadavi-Ardekani does not disclose "a system that allocates shared memory"

271. Dr. Jacobsen's contends that the IDIM disclosed in Fadavi is the claimed shared memory, (Jacobsen Report at Id. at ¶ 371), and that the interleaving and deinterleaving functions in the FCI "share" the IDIM. *See*, Jacobsen Report at ¶¶ 390 and 400. The Court construed shared memory as "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." As explained below, in view of Fadavi's disclosure, the IDIM is not a

common memory used by at least the interleaving and deinterleaving functions, where a portion of the memory can be used by either the interleaving or deinterleaving functions.

272. Fadavi teaches that:

> The size of the IDIM is derived as follows. A simple implementation of a transmit interleaver for G.lite communication requires 4 Kbytes per session for downstream processing, derived by multiplying the maximum codeword length by the maximum interleaver depth. The simple G.lite transmit interleaver also requires 2 Kbytes per session for upstream processing. Therefore, 24 Kbytes of RAM is required to support four G.lite sessions. Similarly, a simple implementation of a transmit interleaver for standard ADSL requires 16 Kbytes per session for downstream processing and 2 Kbytes per session for upstream processing, for a total of 72 Kbytes for four sessions. A fast path buffer is also required for fast path data in both the interleave and de-interleave processes and requires 256 bytes of RAM per session, or a total of 1 Kbytes for four sessions. Since the smallest RAM block currently available is 1Kx16, 1Kx160 or 2 Kbytes must be allocated for the fast path buffer per direction. Therefore, a simple implementation of an interleaver would require 76 Kbytes for four standard ADSL sessions (64 K interleave + 8 K de-interleave + 4 K fast path).

273. Based on the foregoing passage of Fadavi, a POSITA would understand that the size of the IDIM memory depends on the number of sessions/connections that the transceiver is designed to support. Fadavi at 7:6-10 ("**4 Kbytes** per session for downstream processing, . . . **2 Kbytes** per session for upstream processing. Therefore, **24 Kbytes** of RAM [(4+2) x 4] is required to support **four** G.lite sessions."). In an ADSL implementation, the transceiver is equipped with "76 Kbytes for four standard ADSL sessions (64 K interleave +8 K de-interleave +4 K fast path)". *Id.* at 7:23-25. Fadavi explains that the memory sizes are "derived by **multiplying the maximum codeword length by the maximum interleaver depth**." Fadavi at 7:8-10 (emphasis added). Given

that the memory available for interleaving and deinterleaving is the maximum required by the DSL standards, the memory set aside for use by the interleaving function will never be used by the deinterleaving function. Even if the interleaving function uses less than all its memory, because for example, the far-end deinterleaver has lesser memory, the unused memory will not be used by the deinterleaving function because Fadavi contemplates that sufficient memory is set aside for use by the deinterleaver. Accordingly, a POSITA would understand that the IDIM described in Fadavi is not the claimed shared memory.

274. Dr. Jacobsen suggests that the IDIM is the claimed shared memory because Fadavi teaches that the IDIM "may be utilized in a ping-pang fashion." Jacobsen Report at ¶ 371 (citing Fadavi at 6:57-58). I disagree that the ping-pang usage of the IDIM indicates that the IDIM is shared memory. Fadavi explains that ping-pang usage of the IDIM means that "[a]s one area of memory is being used by a first agent, another area of memory can be used by a different agent." Fadavi at 5:60-65. "When the memory is used in ping-pang fashion, '[a]s long as different agents . . . access different areas of a dual access memory, there are no memory address conflicts that could cause communication errors.'" Jacobsen Report at Id. at ¶ 371 (citing Fadavi at 5:65-6:1). Thus, Fadavi merely teaches that the IDIM is a "dual access memory" and that an agent accesses its own area of the IDIM. Thus, although the IDIM is shared between different agents, for the reasons set forth at ¶ 273, the IDIM is not "shared memory," as construed.

275. Fadavi also discloses "[a]n optimal implementation of the interleaver that utilizes the same memory for receive data and transmit data." Fadavi at 7:25-30. To the extent, Dr. Jacobsen suggests that this "optimal implementation" teaches a shared memory, I disagree. The optimal implementation is incompatible with the DSL standards and accordingly a POSITA would not be motivated to use the optimal implementation, much less use the optimal implementation in combination with the G.993.1 standards. *See*, VI.C.6, *infra*.

b. Fadavi-Ardekani in combination with G.993.1 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the interleaver . . . wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"

276. As an initial matter, none of the sections of the G.993.1 standard that Dr. Jacobsen cites between ¶¶ 387-397 of the Jacobsen Report, suggests that a 993.1-compliant VTU-O necessarily includes a shared memory, *i.e.*, "common memory used by at least two functions, where a portion of the memory can be used by either one of the functions." To the extent, Dr. Jacobsen suggests that G.993.1 at § 8.4.1 teaches "allocating a first number of bytes of the shared memory to the interleaver . . ." *See*, Jacobsen Report at ¶ 389, I disagree. § 8.4.1 provides that "[t]he interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255." However, G.993.1 does not disclose or require the use of a "shared memory" by the interleaver and deinterleaver. For example, a transceiver could be designed with a fixed amount of memory that is used for interleaving, where the amount of memory corresponds to the maximum interleave

depth mandated by the standard. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id*. In fact, as described above at § VI.C.2.a, this is precisely the scheme disclosed in Fadavi.

277. Specifically, Fadavi teaches that "[t]he size of the IDIM . . . is derived by multiplying the *maximum codeword length by the maximum interleaver depth*." Fadavi at 7:5-10. Thus, the interleaver in Fadavi is provided with a dedicated amount of memory and the interleaver may use as much as is needed based on the codeword length and interleaver depth. Similarly, the deinterleaver in Fadavi is provided with a dedicated amount of memory and the deinterleaver may use as much as is needed based on the codeword length and interleaver depth. Irrespective of the contents of the initialization messages transmitted or received, no portion of the IDIM set aside for use the interleaving function will ever be allocated for use by the deinterleaving function, and vice versa. And although initialization messages may be exchanged to communicate the capabilities of far-end transceiver, because Fadavi equips each of its interleaver and deinterleaver with the maximum amount of memory contemplated by the standard,

there is no scenario where unused interleaving memory will be allocated for use by the deinterleaver, and vice versa.

278. Dr. Jacobsen incorrectly asserts that "[i]n allocating memory for each of the lines, Fadavi-Ardekani discloses determining the amount of memory to support different sessions required by the transceiver. *See*, Jacobsen Report at ¶ 396 (citing Fadavi at 7:3-33). This is a gross mischaracterization of the cited portion of Fadavi. Fadavi teaches using pre-determined amounts of memory derived by multiplying the *maximum codeword length by the maximum interleaver depth*, as mandated by the relevant standard. Fadavi does teach that "with a lesser depth, additional sessions may be supported with the same size buffer" and "[w]ith a larger buffer, additional session[s] may be supported." Fadavi at 7:30-33. However, this does not suggest that Fadavi allocates shared memory. This merely confirms that Fadavi uses pre-determined amounts of memory per session and precludes any need to use the content of the O-MSG2 message to allocate memory. Accordingly, I disagree with Dr. Jacobsen's assertion at paragraph 396 that a POSITA "would have understood, based on the disclosures of Fadavi-Ardekani, that the allocated memory for the interleaver for each of the supported lines, which would have been determined based on the content of the O-MSG2 message transmitted by the VTU-O corresponding to that line, would not exceed the requirements the VTU-O set for itself in O-MSG2."

279. Based on the foregoing, it is my opinion that the combination of Fadavi and G.993.1 does not disclose this limitation.

c. The combination of Fadavi-Ardekani and G.993.1 does not disclose "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

280. For at least the same reasons set forth in section VI.C.2.b, *supra*, my opinion is that the combination of Fadavi and G.993.1 does not disclose this claim element.

3. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 5 of the '381 patent

a. Fadavi-Ardekani does not disclose "a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

281. At least for the reasons set forth at § VI.C.2.a, Fadavi does not include a "shared memory." Accordingly, Fadavi cannot include "a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for **allocating shared memory in a transceiver.**"

b. Fadavi-Ardekani in combination with G.993.1 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

282. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation. It is noteworthy and worth reiterating that Dr. Jacobsen merely asserts that "[o]ne of ordinary skill in the art would have understood that . . . allocating memory to an interleaver in Fadavi-Ardekani and

G.993,1 apply equally to allocating memory to a deinterleaver." Jacobsen Report at ¶ 142. Dr. Jacobsen does not contend that Fadavi and G.993.1 describe allocating shared memory.

c. Fadavi-Ardekani in combination with G.993.1 does not disclose "allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate"

283. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation.

4. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 13 of the '882 patent

a. Fadavi-Ardekani does not disclose "a system that allocates shared memory"

284. At least for the reasons set forth at § VI.C.2.a, Fadavi does not include a "shared memory." Accordingly, Fadavi does not disclose a system that allocates shared memory.

b. Fadavi-Ardekani in combination with G.993.1 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

285. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation.

c. Fadavi-Ardekani in combination with G.993.1 does not disclose "allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate"

286. At least for the reasons articulated at § VI.C.2.b, the combination of Fadavi and G.993.1 does not disclose this limitation.

5. Fadavi-Ardekani in combination with G.993.1 does not disclose all the limitations of claim 19 of the '473 patent

a. The combination of Fadavi and G.993.1 does not disclose a multicarrier communications transceiver associated with a memory "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

287. Fadavi does not disclose "allocating memory **between** an interleaving function and a deinterleaving function." Dr. Jacobsen contends that the IDIM described in Fadavi is "allocate[ed] between an interleaving function and a deinterleaving function." Jacobsen Report at ¶ 446. I disagree.

288. Dr. Jacobsen states that Fadavi teaches that "[a] portion of the memory is allocated to an interleaver by determining the size of the memory needed to interleave a certain amount of data." Jacobsen Report at ¶ 447. Dr. Jacobsen mischaracterizes Fadavi. The interleaver is assigned a pre-determined amount of memory the size of which "is derived by multiplying the maximum codeword length by the maximum interleaver depth." Fadavi at 7:5-10.

289. Dr. Jacobsen contends that the ping-pang usage of the IDIM means than the "memory is allocated between the interleaving function and the deinterleaving function" Jacobsen Report at ¶ 446. However, the claims require that the allocation of

memory between the interleaving function and the deinterleaving function take place ***in accordance with a message received during initialization***. Dr. Jacobsen has not alleged that such is the case in Fadavi.

290. Dr. Jacobsen also contends that a transceiver can use the parameters specified in the O-MSG2 and R-MSG2 messages described in the G.993.1 standard, "to allocate memory between an interleaver and a deinterleaver." Jacobsen Report at ¶ 447-448. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*). As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

291. Additionally, as previously explained, the transceiver described in Fadavi is designed such that the interleaver and deinterleaver are each provided with a pre-determined amount of memory that equates to the maximum amounts mandated by the standards. If the interleaver uses less than its assigned memory for any reason, the unused memory is not used by the deinterleaver because the deinterleaver is provided with a pre-determined amount of memory that equates to the maximum amount it may require. Thus, the IDIM is not allocated between the interleaving and deinterleaving functions. Accordingly, even if Fadavi is modified to use the O-MSG2 and R-MSG2, the

IDIM would not be "allocated ***between*** the interleaving function and the deinterleaving function in accordance with" these messages.

b. The combination of Fadavi and G.993.1 does not discloses a multicarrier communications transceiver associated with a memory "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

292. Fadavi does not disclose this limitation. As I previously explained, the interleaving and deinterleaving functions in Fadavi are each assigned a pre-determined amount of memory "derived by multiplying the maximum codeword length by the maximum interleaver depth." Fadavi at 7:5-10. Given that each function is provided with its maximum memory requirement, there is no situation where a portion of the memory assigned to the interleaving function may be allocated to the deinterleaving function and vice versa.

293. With respect to the G.993.1 standard, Dr. Jacobsen contends that because "G.993.1 uses Frequency Division Duplexing (FDD)," "data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function." Jacobsen Report at ¶ 452. Based on this, Dr. Jacobsen concludes that "G.993.1 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time." *Id*. I disagree. The claim requires that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." The

claim limitation is not met simply when "a portion of the memory [is] allocated to an interleaving function, and a portion of the memory [is] allocated to a deinterleaving function," as Dr. Jacobsen apparently contends.

294. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.993.1 does not disclose this limitation.

6. A POSITA would not have been motivated to combine Fadavi-Ardekani and G.993.1

295. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 454-459 of the Jacobsen Report that "one of ordinary skill in the art as of the Family 3 patents' priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.993.1 in the manner claimed."

296. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the telecommunications field and relate to DSL systems. *See* Jacobsen Report at ¶ 454. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.C.7 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. That both references are in the telecommunications field is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof. Further, at the time of the inventions of the Family 3 Patents, the DSL standards were under continuous development and there were likely hundreds, if not thousands, of references directed to

possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Fadavi and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

297. I further disagree with Dr. Jacobsen's premise that both Fadavi and G.993.1 describe the need to allocate memory for interleaving and deinterleaving functions. Dr. Jacobsen's opinion that "[o]ne of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions" is not supported by the disclosure of Fadavi. Jacobsen Report at ¶ 456. Contrary to Dr. Jacobsen's assertion, Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory, the size of which is "derived by multiplying the maximum codeword length by the maximum interleaver depth." At least for this reason, a POSITA would not be motivated to modify Fadavi, to allocate memory based on the initialization messages described in G.993.1.

298. Dr. Jacobsen relies on the "optimal implementation of the interleaver" described in Fadavi to demonstrate that Fadavi includes a shared memory. Specifically, Dr. Jacobsen asserts that "Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions." Jacobsen Report at ¶ 372 (citing Fadavi at 7:25-30 ("An optimal implementation of the interleaver according to the

method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth (16 K interleave & de-interleave +4 K fast path).”). It is my opinion that a POSITA would recognize that this implementation would be inoperable with G.993.1.

299. In the optimal implementation, Fadavi discloses that the same memory is used for receive and transmit data, alternately. Data received (deinterleave data) during one cycle will be overwritten by transmit data (interleave data) during a subsequent cycle. The G.993.1 standard requires that “[t]he interleave depth shall be programmable with a maximum interleave depth of 64 codewords when the number of octets per codeword (N) equals 255.” G.993.1 at § 8.4.1. A POSITA would recognize that a codeword, after interleaving, will necessarily span multiple (typically many) DMT frames and that all the DMT frames will not be received during one cycle. Consequently, the deinterleaving operation cannot be completed during that cycle. However, during the next cycle the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted. This means that received data will not be correctly deinterleaved. For this reason, a POSITA would be not have combined the teachings of the G.993.1 and Fadavi.

300. I also disagree with Dr. Jacobsen’s assertion that a skilled artisan would have been motivated to combine the size- and cost-saving approach of Fadavi-Ardekani with the transceivers of G.993.1 to reduce the cost, size, and power consumption of the VTU-Os that would be deployed in optical network units or cabinets. Jacobsen Report at ¶ 457. A POSITA would recognize that modifying Fadavi to use the initialization

messages described in G.993.1 would add to complexity. Further, in view of that fact that the memory sizes in Fadavi are "derived by multiplying the maximum codeword length by the maximum interleaver depth," processing and using the initialization messages of G.993.1 would bring no benefit to Fadavi.

301. For these reasons, a POSITA would not be motivated to combine the teachings of Fadavi and G.993.1.

D. The Asserted Claims Are Not Obvious Over Fadavi-Ardekani in Combination with ITU-T Recommendation G.992.2

1. Fadavi-Ardekani in combination with G.992.1 does not disclose all the limitations of claim 1 of the '048 patent

a. Fadavi-Ardekani does not disclose "a system that allocates shared memory"

302. For the reasons set forth at § VI.C.2.a, Fadavi-Ardekani does not disclose "a system that allocates shared memory."

b. Fadavi-Ardekani in combination with G.992.2 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the interleaver . . . wherein the allocated memory for the interleaver does not exceed the maximum number of bytes specified in the message"

303. For the reasons set forth at § VI.C.2.b, I disagree that Fadavi's system includes the capability to "allocat[e] a first number of bytes of the shared memory to a interleaver" much less the capability to "allocat[e] a first number of bytes of the shared memory" such that "the allocated memory . . . does not exceed the maximum number of bytes specified in the message."

304. Separately, Dr. Jacobsen contends that C-RATES1, R-RATES1, C-RATES-RA, R-RATES2 and C-RATES2 messages "can be used to allocate memory to

implement" the interleaver. However, Dr. Jacobsen neglects to consider the plain meaning of the claims. The claims require allocating bytes of the shared memory, where the shared memory is "common memory used by at least two functions where a portion of the memory can be used by either one of the functions." Like the G.993.1 standard, the G.992.2 standard does not require that a transceiver implement a "shared memory" much less "allocat[e] a first number of bytes of **the shared memory** to an interleaver." Rather, a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.* Accordingly, the combination of Fadavi and the G.992.2 does not disclose this claim limitation.

c. Fadavi-Ardekani in combination with G.992.2 does not disclose "allocating a second number of bytes of the shared memory to a deinterleaver to deinterleave a second plurality of RS coded data bytes received at a second data rate"

305. For at least the same reasons set forth at § VI.D.1.b, my opinion is that the combination of Fadavi and G.992.2 does not disclose this claim element.

2. Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitations of claim 5 of the '381 patent

a. Fadavi-Ardekani does not disclose "a non-transitory computer-readable information storage media having stored thereon instructions, that if executed by a processor, cause to be performed a method for allocating shared memory in a transceiver"

306. At least for the reasons set forth at §§ VI.C.2.a and C.3.a, Fadavi does not disclose this element.

b. Fadavi-Ardekani in combination with G.992.2 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

307. For the reasons set forth at § VI.D.1.b, the combination of Fadavi and G.992.2 does not disclose this element.

c. Fadavi-Ardekani in combination with G.992.2 does not disclose "allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate"

308. For the reasons set forth at § VI.D.1.b, the combination of Fadavi and G.992.2 does not disclose this element.

3. Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitation of claim 13 of the '882 patent

a. Fadavi-Ardekani does not disclose "a system that allocates shared memory"

309. For the reasons set forth at § VI.C.2.a, Fadavi-Ardekani does not disclose "a system that allocates shared memory."

b. Fadavi-Ardekani in combination with G.992.2 does not disclose "a transceiver capable of . . . allocating a first number of bytes of the shared memory to the deinterleaver . . . wherein the allocated memory for the deinterleaver does not exceed the maximum number of bytes specified in the message"

310. For the reasons set forth at § VI.D.1.b, the combination of Fadavi and G.992.2 does not disclose this element.

c. Fadavi-Ardekani in combination with G.992.2 does not disclose "allocating a second number of bytes of the shared memory to a interleaver to interleave a second plurality of RS coded data bytes received at a second data rate"

311. For the reasons set forth at § VI.D.1.b, the combination of Fadavi and G.992.2 does not disclose this element.

4. Fadavi-Ardekani in combination with G.992.2 does not disclose all the limitation of claim 19 of the '473 patent

a. The combination of Fadavi and G.992.2 does not disclose a multicarrier communications transceiver associated with a memory "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

312. For the reasons set forth at § VI.C.5.a, Fadavi does not disclose this element. Separately, the G.992.2 standard does not disclose this limitation. Dr. Jacobsen contends that certain initialization messages "**can be used** to allocate memory between an interleaver and a deinterleaver." Jacobsen Report at ¶ 524. The G.992.2 standard, however, does not teach using the initialization messages to allocate memory between an interleaver and a deinterleaver. Rather, a POSITA would understand G.992.2 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated

memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

b. The combination of Fadavi and G.992.2 does not discloses a multicarrier communications transceiver associated with a memory "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

313. Fadavi does not disclose this limitation. See § VI.C.5.b.

314. With respect to the G.992.2 standard, Dr. Jacobsen contends that because G.992.2 establishes a "single duplex bearer channel," one of ordinary skill in the art would have understood that data is transmitted in both directions at the same time and as a result, the interleaver and deinterleaver are both used at the same time. Jacobsen Report at ¶ 526. Based on this, Dr. Jacobsen concludes that G.992.2 discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time. *Id*. I disagree. The claim requires that "at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." The claim limitation is not met simply when a portion of the memory is allocated to an interleaving function, and a portion of the memory is allocated to a deinterleaving function.," as Dr. Jacobsen apparently contends.

315. Accordingly, it is my opinion that the combination of Fadavi-Ardekani and G.992.2 does not disclose this limitation.

5. A POSITA would not have been motivated to combine Fadavi-Ardekani and G.992.2

316. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 527-531 of the Jacobsen Report that "one of ordinary skill in the art as of the Family 3 patents' priority date would have been motivated to combine the teachings of Fadavi-Ardekani with the teachings of G.992.2 in the manner claimed."

317. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the telecommunications field and relate to ADSL systems. *See* Jacobsen Report at ¶ 527. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.D.6 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. That both references are in the telecommunications field is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof. Further, at the time of the inventions of the Family 3 Patents, the DSL standards were under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would

provide no useful benefit. Thus, that Fadavi and G.992.2 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

318. I further disagree with Dr. Jacobsen's premise that both Fadavi and G.992.2 describe the need to allocate memory for interleaving and deinterleaving functions. Dr. Jacobsen opinion that "[o]ne of ordinary skill in the art naturally would have consulted Fadavi-Ardekani for its description of calculating memory needs and allocating memory between interleaver and deinterleaver functions" is not supported by the disclosure of Fadavi. Jacobsen Report at ¶ 528. Contrary to Dr. Jacobsen's assertion, Fadavi merely teaches providing each interleaver and deinterleaver with a dedicated amount of memory, the size of which is "derived by multiplying the maximum codeword length by the maximum interleaver depth." At least for this reason, a POSITA would not be motivated to modify Fadavi, to allocate memory based on the initialization messages described in G.992.2.

319. Dr. Jacobsen relies on the "optimal implementation of the interleaver" described in Fadavi to demonstrate that Fadavi includes a shared memory. Specifically, Dr. Jacobsen asserts that "Fadavi-Ardekani further describes allocating the IDIM memory between transmit and receive functions." Jacobsen Report at ¶ 372 (citing Fadavi at 7:25-30 ("An optimal implementation of the interleaver according to the method of the invention utilizes the same memory for receive data and transmit data and thus requires 20 Kbytes to support a standard ADSL session at full interleave depth

(16 K interleave & de-interleave +4 K fast path)."). It is my opinion that a POSITA would recognize that this implementation would be inoperable with G.992.2.

320. In the optimal implementation, Fadavi discloses that the same memory is used for receive and transmit data, alternately. Data received (deinterleave data) during one cycle will be overwritten by transmit data (interleave data) during a subsequent cycle. The G.992.2 standard requires that "The Reed-Solomon codewords shall be convolutionally interleaved." G.992.2 at § 7.6. A POSITA would recognize that a codeword, after interleaving, will necessarily span multiple (typically many) DMT frames and that all the DMT frames will not be received during one cycle. Consequently, the deinterleaving operation cannot be completed during that cycle. However, during the next cycle the received deinterleave data will be overwritten with interleave data that must be interleaved and transmitted. This means that received data will not be correctly deinterleaved. For this reason, a POSITA will be dissuaded from combining the teachings of the G.992.2 and Fadavi.

321. Separately, a POSITA would recognize that modifying Fadavi to use the initialization messages described in G.992.2 would add to complexity. Further, in view of that fact that the memory sizes in Fadavi are "derived by multiplying the maximum codeword length by the maximum interleaver depth," processing and using the initialization messages of G.992.2 would bring no benefit to Fadavi.

322. For these reasons, a POSITA would not be motivated to combine the teachings of Fadavi and G.992.2.

E. Claim 19 of the '473 Patent Is Not Obvious Over Voith in Combination with LB-031

323. It is my opinion and conclusion that Voith alone or in combination with LB-031 fails to disclose or suggest each element of the claim 19 of the '473 patent, and hence fails to render the claim 19 of the '473 patent obvious as described in detail, below.

324. It is also my opinion that regardless of the disclosures of Voith and LB-031 individually, a person of ordinary skill in the art would not be motivated to combine the teachings of Voith with the teachings of LB-031 at least for the reasons described in Section VI.E.3, *infra*.

325. An overview of LB-031 has been provided in Section VI.A.1, *supra.*

1. Neither Voith nor LB-031 discloses a multicarrier communications transceiver associated with a memory "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

326. Dr. Jacobsen contends that "Voith discloses allocating memory between the interleaving function and the dinterleaving (sic) function" because Voith states that the interleaver "uses a portion of external interleave/deinterleave memory 66." Jacobsen Report at ¶ 557 (citing Voith at 5:65-61). This is not correct. It does not follow from the fact that the external memory is used for both interleaving and deinterleaving that any portion of the memory is allocated ***between*** these functions.

327. Dr. Jacobsen has not shown that any portion of the interleave/deinterleave memory 66 is disclosed by Voith to be used as interleaver memory at one point in time and deinterleaver memory at another point in time.

Therefore, there is no basis for concluding that Voith allocates memory between an interleaving function and a deinterleaving function. Rather, a POSITA reviewing Voith's disclosure of an external interleave/deinterleave memory 66, would understand this as disclosing that the memory includes a dedicated portion for use by interleaver 78 and a separate, dedicated portion for use by deinterleaver 90. Such a predetermined division of separate, dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, supra. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

328. Further, Voith does not disclose performing any allocation of interleaver or deinterleaver memory "in accordance with a message received during an initialization of the transceiver." The only reference to a "message" in Dr. Jacobsen analysis for this claim element is the single conclusory sentence that "the bit allocation table is determined during initialization by the receiving transceiver and communicated to the transmitting transceiver in a message sent during the initialization procedure." Jacobsen Report at ¶ 558. Dr. Jacobsen appears to be relying on a message such as the O-B&G message described in the G.993.1 standard (§ 12.4.6.2.1.3 ("O-B&G shall signal the end of the contract negotiation and shall be used to transmit to the VTU-R the bits and the gains information that are to be used in the upstream direction.")) or the C-B&G message described in the G.992.2 standard (§ 11.11.13) as a message used for the

claimed memory allocation. However, Dr. Jacobsen provides no evidence that Voith teaches that ADSL transceiver 34 allocates memory 66 between the interleaver 78 and the deinterleaver 90 based on a bit-allocation message. Accordingly, I disagree that "Voith discloses wherein the ***memory is allocated*** between the interleaving function and the deinterleaving function ***in accordance with a message received during an initialization of the transceiver***," as Dr. Jacobsen alleges. Jacobsen Report at ¶ 558.

329. With respect to LB-031, as I previously explained at § VI.A.5.a, *supra*, LB-031 does not disclose this element. Specifically, LB-031 only teaches that the "VTU-O and VTU-R would then select the smaller of the transmitter and receiver capabilities in each direction, as the end-to-end capabilities." LB-031 at p. 3. Accordingly, LB-031 at most discloses that a VTU-O (or a VTU-R) determines whether it can use all of its predetermined maximum interleaver memory or whether it has to use less of it because of the maximum capabilities of the deinterleaver on the other side of the line, are smaller. However, LB-031 does not teach that the unused portion of the interleaver memory can be allocated to the deinterleaver. Accordingly, LB-031 does not teach "the memory is allocated ***between*** the interleaving function and the deinterleaving function depending on a message."

330. Accordingly, it is my opinion that neither Voith nor LB-031, alone or in combination, discloses this limitation.

2. Neither Voith nor LB-031 discloses a multicarrier communications transceiver associated with a memory "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

331. Voith does not disclose this limitation. Voith merely teaches that a first portion of memory 66 is used by the interleaver 78 and a second portion of memory 66 is used by the deinterleaver 90. Voith does not teach that this apportioning is performed based on a message. *See* Supra at ¶ 367. Additionally, Voith does not teach that any portion of the memory 66 may be allocated to the interleaver 78 ***or*** the deinterleaver 90 at any one particular time depending on a message.

332. Dr. Jacobsen has not pointed to any disclosure or teaching in Voith that states, or necessarily requires, that it uses memory where any portion is shared between an interleaving function and a deinterleaving function. Rather, a POSITA reviewing Voith's disclosure of an external interleave/deinterleave memory 66, would understand this as disclosing that the memory includes a dedicated portion for use by interleaver 78 and a separate, dedicated portion for use by deinterleaver 90. Such a predetermined division of separate, dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

333. Dr. Jacobsen asserts that a POSITA would interpret Voith, including the sentences "[i]nterleaver 78 arbitrates for use of external interleave/deinterleave memory 66 with the deinterleaver 90" (Voith at 6:1-4) and "deinterleaver 90 makes use of external interleave/deinterleave memory 66 and arbitrates for usage thereof in a manner similar to interleaver 78" (*id.* at 26-29), as disclosing that "a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time." Jacobsen Report at ¶¶ 557 and 562. I disagree. These sentences only mean that the interleaver 78 and deinterleaver 90 contend for access to the "external memory interface" in order to access external memory 66. Such contention for access to the external memory interface in general does not indicate in any way that the interleaver 78 and deinterleaver 90 are contending for or using, or capable of contending for or using, the same portions of the memory.

334. With reference to LB-031, for the same reasons set forth above at VI.A.5.a and b, *supra*, LB-031 does not disclose this limitation.

3. No Motivation to Combine Voith with LB-031

335. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 566-568 of the Jacobsen Report that "one of ordinary skill in the art would have been motivated to combine Voith and LB-031."

336. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are "in the telecommunications field." Jacobsen Report at ¶ 566. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.E.3 of the Jacobsen Report, is not sufficient show that a person of

ordinary skill in the art would have combined the teachings of the two references. This is simply far too broad and general of a field to say that that a POSITA would be motivated to combine any one of the many thousands of diverse telecommunications techniques, or any particular feature or function thereof.

337. Dr. Jacobsen further asserts that there is a motivation to combine because each of the references purportedly "discloses sharing memory for interleaving and deinterleaving to support various applications." *Id.* at ¶ 566. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.E.3 of the Jacobsen Report, is not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references.

338. Also, this assertion is not accurate. As explained in VI.A.1, *supra*, LB-031 is concerned with providing a solution that meets certain delay requirements specified in units of time, while allowing use of larger dedicated interleaver or deinterleaver memories if both transceivers support more than the minimum required by a standard. There is no technique described in LB-031 for "sharing memory for interleaving and deinterleaving to support various applications," contrary to Dr. Jacobsen assertions. *See* § VI.A.1., *supra*. Rather, as I explained above, LB-031 describes a dedicated interleaver memory and a separate, dedicated deinterleaver memory where portions of a dedicated memory that is left unused by one function – because one transceiver supports more memory for a given latency path than is supported by the other transceiver with which it is communicating – is not available for use by the other function.. *See* § VI.A.5.a and ¶¶ 169-178, *supra*.

339. Voith also does not disclose "sharing memory for interleaving and deinterleaving to support various applications." Jacobsen Report at ¶ 567. Voith merely teaches that it is preferable to implement the memory buffers off-chip, because "large buffers consume a large integrated circuit are which adds to cost." Voith at 2:27-28. Thus, Voith's fundamental premise is to concede that the memory buffers are required to be large but Voith makes no proposal for reducing such requirement. Voith certainly does not propose the use of sharing memory for interleaving and deinterleaving where a portion of the memory can be used at one time for interleaving and at another time for deinterleaving as explained immediately above in sections VI.E.1 and 2.

340. Therefore, it is my opinion that a POSITA would not be motivated to combine Voith and LB-031, particularly not in any manner "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

F. Claim 19 of the '473 Patent Is Not Obvious Over Mazzoni and G.993.1

1. A Person of Ordinary Skill in the Art Would Not Combine the Teachings of Mazzoni with the Teachings of G.993.1

341. A person of ordinary skill in the art at the time of the invention of the Family 3 Patents would not look to the teachings of Mazzoni when implementing the teachings of G.993.1, or *vice versa*. In fact, as explained below, the two references are so different that a person of ordinary skill in the art would be discouraged from looking to the teaching of the other reference.

342. The overview of Mazzoni has been provided in Section VI.B.1, *supra*.

343. G.993.1, akin to LB-031, is yet another reference that employs a dedicated interleaver memory and a dedicated deinterleaver memory. Dr. Jacobsen relies on G.993.1 for its "initialization message scheme." *See* Jacobsen Report at ¶ 595.

344. Dr. Jacobsen asserts that a reason to combine Mazzoni and G.993.1 is that both are "directed to VDSL and to VDSL transceivers." *See* Jacobsen Report at ¶ 592. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.F.4 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the VDSL standard was still under development and there were likely hundreds of references directed to possible implementation details of many and varied proposals for VDSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni and G.993.1 are both directed to different proposals for developing VDSL transceivers, would not have made their combination obvious.

345. Dr. Jacobsen then states that "each of Mazzoni and G.993.1 discloses a need to allocate memory for interleaving and deinterleaving." *See* Jacobsen Report at ¶ 593. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section VIII.F.4 of the Jacobsen Report, is again not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the two references. It is far too general of a concept to provide any motivation to combine one reference with the

other. In fact, it is not materially different than saying that Mazzoni and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

346. Dr. Jacobsen states that: "[a]s a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers. One of ordinary skill in the art would have recognized that conveying interleaver parameters through initialization message scheme of G.993.1 would avoid this limitation of Mazzoni's table and would result in a more flexible solution." *See* Jacobsen Report at ¶ 595. This is incorrect.

347. A POSITA would not look to add a message (from G.993.1 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I', and M' parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. *See* Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the maximum supported interleaver or deinterleaver memory size because all data rate pairs and their corresponding I, M, I', and M' values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant and serve no useful purpose.

348. "Flexibility" is also too generic of a motivation to combine and, in any event, Mazzoni provides substantial flexibility already given that it allows 12 difference service configurations. One of skill in the art who perceived the benefits of the simplicity of configuration that Mazzoni provides would not be motivated to use the complex messaging and initialization scheme of G.993.1.

349. An additional reason why G.993.1's exchange of maximum supported memory sizes would not be recognized as beneficial to Mazzoni is that it is incompatible. For example, per G.993.1, the VTU-R (i.e., TR of Mazzoni) transmits to the VTU-O (i.e., TU of Mazzoni) an R-MSG2 message that specifies the maximum downstream deinterleaver memory size that it supports. Then the VTU-O transmits to the VTU-R an O-MSG2 message that specifies the maximum upstream interleaver memory size it can support. Using the predefined services described in Mazzoni, i.e., S1-S6 and A1-A6 (*see* Mazzoni at 3:62 – 4:14), the maximum downstream deinterleaver memory that Mazzoni is capable of supporting is determined by reference to the A6 service and the maximum upstream interleaver memory that Mazzoni is capable of supporting is determined by reference to the S6 service. The A6 service provides a downstream bit rate of 832x64 kbit/s and requires 24,960 bytes of deinterleaver memory. *See id.* at 6:11-30 (describing calculation of required deinterleaver memory size). The S6 service provides an upstream bit rate of 362x64 kbit/s. Per the calculations described at 6:11-30 of Mazzoni, the S6 service requires that the VTU-R be capable of supporting a maximum upstream interleaver memory of 10,860 bytes. If the Mazzoni VTU-O received a message indicating that the VTU-R supported a maximum

downstream deinterleaver memory of 24,960 bytes and a maximum upstream interleaver memory of 10,860 bytes (based on the maximum interleaver delay), this information would be useless to the VTU-O. First, it already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation. Second, neither the VTU-O or VTU-R would actually be capable of simultaneously supporting both maximum interleaver and deinterleaver sizes at the same time because the total memory size of the Mazzoni transceivers is only 26,890 bytes (as determined by the combined upstream and downstream bit rates of the A6 service). *See id.* at 4:18-22 and 6:45-50.

350. Further, while Dr. Jacobsen does not put forth any argument regarding any other messages in her report (I reserve the right to respond to any such new argument to the extent she is allowed to raise it), per G.993.1, after the exchange of the R-MSG2 and the O-MSG2 messages, the VTU-R transmits an R-CONTRACT1 message to the VTU-O including a "proposed downstream contract." Subsequently, the VTU-O transmits the O-CINTRACT1 message to the VTU-R which contains a proposed upstream contract and a downstream contract, where the downstream contract is based on the R-CONTRACT1. Again, Mazzoni already has the information necessary to support the service for which both transceivers have been preconfigured at the time of installation and does not need to rely on messages to convey the redundant information.

351. A POSITA at the time of the Family 3 Patent inventions would not combine the teachings of Mazzoni with the teachings of G.993.1. If fact, a POSITA would be discouraged from doing so. Because Mazzoni teaches that an assignment of the memory is performed at the time of the installation of the modem based on a table, and not a message, adding a message (or multiple messages) to this system per G.993.1 would be unnecessary, redundant, and create useless complexity during initialization. Further, because Mazzoni is concerned with supporting a finite set of predefined service configurations (i.e., data rate pairs and corresponding interleaver/deinterleaver parameter values).

352. For at least the foregoing reasons, Dr. Jacobsen has not demonstrated that a POSITA would have been motived to combine G.993.1 with Mazzoni in the manner she proposes.

2. The Combination of Mazzoni and G.993.1 Does Not Render Claim 19 of the '473 Patent Obvious

353. It is my opinion for the reasons provided in Section VI.F.1 above and as further discussed in this Section VI.F.2, that a POSITA would not combine Mazzoni and G.993.1 or arrive at the claimed invention even if one were to attempt to combine these references in some way. It is further my opinion and conclusion that Mazzoni in combination with G.993.1 fails to disclose each element of claim 19 of the '473 patent, and hence fails to render claim 19 of the '473 patent obvious as described in detail, below.

a. The Combination of Mazzoni and G.993.1 does not disclose a multicarrier transceiver being associated with a memory wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver.

354. Mazzoni in combination with G.993.1 does not disclose this limitation. Dr. Jacobsen incorporates by reference her arguments with respect to Mazzoni by pointing to Section IX.B.6.e of the Jacobsen Report. These arguments have been addressed in Section VI.B.6.a, *supra* and further below.

355. Dr. Jacobsen then points to Section IX.C.6.e of the Jacobsen Report for support that "G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver." Dr. Jacobsen does not explain which of her arguments in the cited section are applicable to this new combination. Nor does Dr. Jacobsen address the "ways of allocating memory between an interleaver and a deinterleaver" in G.993.1 in this or the cited section. I reserve the right to address any support or explanation Dr. Jacobsen's attempts to provide for her currently conclusory assertions regarding this combination of references.

356. Nonetheless, looking back at the cited Section IX.C.6.c from the Jacobsen Report, Dr. Jacobsen describes the R-MSG2 and the O-MSG2 messages in paragraphs 447-448. As I explained in Section VI.F.1, *supra*, G.993.1's exchange of interleaver and deinterleaver capabilities though those messages is redundant to Mazzoni's stored predefined service data rates and interleaver/deinterleaver parameters and incompatible with Mazzoni at least because the exchange of maximum supported

interleaver and deinterleaver sizes per G.993.1 would specify a combined amount of interleaver and deinterleaver memory that would exceed Mazzoni's total memory size.

357. Further with respect to Mazzoni, looking back at what Dr. Jacobsen incorporates by reference, contrary to her opinion, Mazzoni does not disclose exchanging any messages at all that includes information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would have understood that this information, as well as capabilities of the transceiver at the other end of the system, would have to be conveyed, for example, in the form of a message during initialization, and that the memory would be allocated between the interleaving function and the deinterleaving function in accordance with that message." Jacobsen Report at ¶ 339. The "information" she is referring to is the parameters I, M, I' and M'. But, she cannot point to any disclosure of such a message in Mazzoni because there is no such disclosure. Instead, it seems that she is interpreting Mazzoni's description of the configurability of its interleaver means and deinterleaver means according to upstream and downstream bit rates as somehow disclosing reliance on an exchange of I, M, I' and M'. *See id.* (citing Mazzoni at 1:61-65 and 5:24-31). But parameters I, M, I' and M' are not exchanged in any message; rather, as discussed above in Section VI.B.1, *supra*, these parameters are stored in a table in each transceiver and indexed to a predefined service that includes predefined upstream and downstream bit rates. Mazzoni at 6:53-61. The parameter values for the particular predefined service are retrieved by the control means MCD at

the time the modem is installed (*id.*) and delivered by the MCD to the interleaver means MET and deinterleaver means MDET (*id.* at 5:21-23 and Fig. 3). This eliminates any need to exchange these parameters between modems.

358. One of the passages Dr. Jacobsen cites for this assertion (again in the section incorporated by reference), Mazzoni at column 5:24-31, does not describe some alternative embodiment where the I, M, I′ and M′ parameters are exchanged in messages. Rather, this passage simply describes the use of the predetermined parameters that are indexed to the predetermined service bit rates the transceiver has been configured to use. Dr. Jacobsen accurately admits this in her report when addressing the purported motivation to combine Mazzoni and G.993.1. *See, e.g.*, Jacobsen Report at ¶ 595 ("Mazzoni discloses keeping a table of values of the interleaver parameters, indexed by service identifiers, in the transceiver. *See id.* at col. 6:51-61. As a person having ordinary skill in the art as of the '473 patent's priority date would have understood, Mazzoni's table is limiting in that all of the services would have to be identified ahead of time and stored in the transceivers."); *see also id.* at ¶ 626.

359. The other passage Dr. Jacobsen relies on for this assertion, Mazzoni at column 1:61-65, also does not disclose or require the exchange of any interleaver or deinterleaver parameters in a message. To the extent Dr. Jacobsen is interpreting this passage as disclosing anything other than the use of predetermined parameters that correspond to predetermined bit rates, she has misunderstood Mazzoni. In fact, the sentence after the one she quotes shows that the reference to "the bit rate actually processed by the send/receive device (modem)" is referring to one of the

predetermined bit rates for a predetermined service. Mazonni at 1:65 – 2:2 ("The invention therefore provides a device for sending/receiving digital data that is capable of ***processing different bit rates from a group of predetermined bit rates*** (e.g., all the symmetrical or asymmetrical services offered by the VDSL communication system)."). Therefore, Mazzoni does not, and need not, rely on any messages to carry out its suggested implementation. In fact, a POSITA would be discouraged to look to any references disclosing messages as described above.

360. Accordingly, the combination of G.993.1 and Mazzoni does not disclose "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver" and, at least for this reason, claim 19 of the '473 patent is not obvious in view of LB-031 and Mazzoni.

b. The combination of Mazzoni and G.993.1 does not disclose a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message.

361. For the reasons discussed immediately above and in Sections VI.F.1 and VI.B.6.b, *supra*, Mazzoni does not disclose this claim element.

362. Dr. Jacobsen incorporates her arguments regarding Mazzoni from "Section (sic paragraph) 339." Yet, this paragraph does not address what Dr. Jacobsen asserts it does. Nonetheless, Dr. Jacobsen's arguments from this paragraph have been addressed in VI.B.6.a, *supra*. I also incorporate my arguments regarding Mazzoni from Section VI.B.6.b, *supra*. In summary, as I explained in the section immediately above,

Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory allocations could be based). Further, as I explained in the section immediately above and in Section VI.F.1, *supra*, G.993.1's exchange of interleaver and deinterleaver capabilities is redundant to and incompatible with Mazzoni.

363. With respect to G.993.1, Dr. Jacobsen cites to Section IX.C.6.f. Dr. Jacobsen's conclusion in paragraph 452 of that section of the Jacobsen Report states that "[o]ne of ordinary skill in the art would have understood that data would need to be interleaved and deinterleaved at the same time in this mode of transmission, which would require that a portion of the memory be allocated to an interleaving function, and a portion of the memory would be allocated to a deinterleaving function." This is incorrect. That an interleaver and deinterleaver operate at the same time does not disclose or require that a portion of the memory be allocated to the interleaver function or deinterleaver function at any one particular time depending on the message. Perhaps this was a cut and paste error and was intended for the element of claim 5 of the '381 patent, which recites: "wherein the shared memory allocated to the deinterleaver is used at the same time as the shared memory allocated to the interleaver."

364. For at least the foregoing reasons, the combination of Mazzoni and G.993.1 does not disclose "a multicarrier transceiver being associated with a memory wherein at least a portion of the memory may be allocated to the interleaving function or the

deinterleaving function at any one particular time depending on the message" and, at least for this reason, claim 19 of the '473 patent is not obvious in view of Mazzoni and G.993.1.

G. Claim 19 of the '473 Patent Is Not Obvious Over Voith and G.993.1, or, In the Alternative, In View of Voith, G.993.1 and Mazzoni

365. It is my opinion and conclusion that Voith alone or in combination with G.993.1 fails to disclose or suggest each element of the claim 19 of the '473 patent, and hence fails to render the claim 19 of the '473 patent obvious as described in detail, below.

366. It is also my opinion that regardless of the disclosures of Voith and G.993.1 individually, a person of ordinary skill in the art would not be motivated to combine the teachings of Voith with the teachings of G.993.1 at least for the reasons described in Section VI.F.3, *supra.*

1. Neither Voith nor G.993.1 discloses a multicarrier communications transceiver associated with a memory "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver"

367. Voith does not disclose this limitation as discussed in section VI.E.1, *supra.*

368. Dr. Jacobsen refers to Section IX.C.6.e of the Jacobsen Report and contends that "G.993.1 teaches sending messages during initialization that indicate maximum interleaver delay, as well as ways of allocating memory between an interleaver and a deinterleaver." Jacobsen Report at ¶ 611. As an initial matter, Dr, Jacobsen has provided no evidence for her assertion that the G.993.1 standard teaches "allocating memory between an interleaver and a deinterleaver" much less "allocating memory

between an interleaver and a deinterleaver in accordance with a message received during an initialization" based on a message received during initialization. Rather, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other ADSL and G.Lite-compliant modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

369. Assuming for the sake of argument that the G.993.1 message identified by Dr. Jacobsen indicates a "maximum interleaver delay," nothing in the G.993.1 standard suggests "allocating memory between an interleaver and a deinterleaver in accordance," with the "maximum interleaver delay." Again, given the state of DSL transceivers during the relevant time frame and the maximum data rates specified by the G.993.1, there is no basis for assuming that DSL transceivers implementing G.993.1 would have used anything other than dedicated, separate interleaver and deinterleaver memories. A POSITA would have understood that the interleaver of a G.993.1-complaint transceiver may have used less than all of its dedicated interleaver memory based on the memory capabilities of the far-end transceiver's deinterleaving function. However, the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver.

370. At least for these reasons, Voith and G.993.1 do not teach a transceiver "wherein the memory is allocated between the interleaving function and the deinterleaving function in accordance with a message received during an initialization of the transceiver."

2. Neither Voith nor G.993.1 discloses a multicarrier communications transceiver associated with a memory "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message"

371. Voith does not disclose this limitation as discussed in section VI.E.2, *supra*.

372. With reference to G.993.1, for the same reasons set forth above at § VI.C.5.b, my opinion is that G.993.1 does not disclose this limitation. Additionally, as discussed in the section immediately above, there is no basis for assuming that DSL transceivers implementing G.993.1 would have used anything other than dedicated, separate interleaver and deinterleaver memories. Rather, a POSITA would have understood that the interleaver of a G.993.1-complaint transceiver may have used less than all of its dedicated interleaver memory but the transceiver would not have been capable of reallocating the unused interleaver memory to its deinterleaver. Thus, no portion of any memory could be allocated to an interleaving function at one time and to a deinterleaving function at another time.

373. At least for these reasons, Voith and G.993.1 do not teach a transceiver "wherein at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message."

3. No Motivation to Combine Voith with G.993.1

374. For the following reasons, I disagree with Dr. Jacobsen's assertion at paragraphs 566-568 of the Jacobsen Report that "one of ordinary skill in the art would have been motivated to combine Voith and G.993.1."

375. First, Dr. Jacobsen asserts that that there is a motivation to combine because both references are in the DSL field. *See* Jacobsen Report at ¶ 617. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.3 of the Jacobsen Report, is not sufficient show that a person of ordinary skill in the art would have combined the teachings of the two references. At the time of the invention of the Family 3 Patents, the DSL standard have been under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Voith and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

376. Dr. Jacobsen further asserts that there is a motivation to combine because each of the references purportedly "discloses a need to allocate memory for interleaving and deinterleaving." *Id.* at ¶ 617. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.3 of the Jacobsen Report, is not sufficient to motivate a person of ordinary skill in the art to combine the teaching of the

two references. It is far too general of a concept to provide any motivation to combine one reference with the other. In fact, it is not materially different than saying that Voith and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

377. I also disagree with Dr. Jacobsen's assertion that there is a motivation to combine Voith and G.993.1 because they purportedly both relate to "allocating memory for interleaving and deinterleaving to support various applications." Jacobsen Report at ¶ 618.

378. With reference to Voith, Dr. Jacobsen asserts that Voith's recognition that "ADSL transceiver 34 requires a large amount of memory, which is preferably implemented off-chip in external interleave/de-interleave memory 66" somehow means that Voith "discloses a need to allocate memory for interleaving and deinterleaving." Jacobsen Report at ¶ 617. I disagree with this assertion. Voith merely teaches that it is preferable to implement the memory buffers off-chip, because "large buffers consume a large integrated circuit are which adds to cost." Voith at 2:27-28. Thus, Voith's fundamental premise is to concede that the memory buffers are required to be large but Voith makes no proposal for reducing such requirement. Voith certainly does not propose the use of sharing memory for interleaving and deinterleaving where a portion of the memory can be used at one time for interleaving and at another time for deinterleaving as explained immediately above sections VI.E.1 and 2.

379. With reference to the G.993.1 standard, Dr. Jacobsen asserts that "[o]ne of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Voith to partition the

shared memory between the interleaver and deinterleaver." Jacobsen Report at ¶ 619. I disagree, there is no disclosure or suggestion in G.993.1 of using or partitioning shared memory. Dr. Jacobsen does not cite any portion of G.993.1 as purportedly disclosing this. On the contrary, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other DSL modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

380. Therefore, it is my opinion that a POSITA would not have been motivated to combine Voith and G.993.1 in the manner proposed by Dr. Jacobsen, and Dr. Jacobsen has not shown otherwise.

4. Mazzoni does not Supply the Disclosure Missing from G.993.1 and Voith

381. Dr. Jacobsen contends that "Mazzoni discloses that at least a portion of the memory may be allocated to the interleaving function or the deinterleaving function at any one particular time depending on the message." Jacobsen Report at ¶ 623. Contrary to Dr. Jacobsen's opinion, Mazzoni does not disclose exchanging any messages at all that include information about interleaving or deinterleaving parameters (or any other information upon which interleaver or deinterleaver memory

allocations could be based). I incorporate by reference my opinions set forth at §§ VI.B.6.a and VI.B.6.b for why Mazzoni does not disclose this element of the claim.

5. A POSITA would not be Motivated to Combine Mazzoni with Voith and G.993.1

382. Contrary to Dr. Jacobsen's assertion, a POSITA would not be motivated to combine Mazzoni with Voith and G.993.1. First, Dr. Jacobsen asserts that that there is a motivation to combine because these references are "in the DSL field." Jacobsen Report at ¶ 625. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.5 of the Jacobsen Report, is not sufficient to show that a person of ordinary skill in the art would have combined the teachings of the three references. At the time of the invention of the Family 3 Patents, the DSL standard have been under continuous development and there were likely hundreds, if not thousands, of references directed to possible implementation details of many and varied proposals for DSL transceivers. One of skill in the art at the time would have understood that many of these references would be completely incompatible with one another and/or, if combined, would provide no useful benefit. Thus, that Mazzoni, Voith and G.993.1 are purportedly both directed to different proposals for DSL transceivers, would not have made their combination obvious.

383. Dr. Jacobsen also contends that "[l]ike Voith and G.993.1, Mazzoni describes a need to allocate memory for interleaving and deinterleaving." *See* Jacobsen Report at ¶ 625. This in and of itself, or in combination with any other argument made by Dr. Jacobsen in Section IX.G.5 of the Jacobsen Report, is again not sufficient to

motivate a person of ordinary skill in the art to combine the teaching of the three references. It is far too general of a concept to provide any motivation to combine one reference with the other. In fact, it is not materially different than saying that Mazzoni, Voith and G.993.1 contemplate the use of memories for interleaving and deinterleaving.

384. I also disagree with Dr. Jacobsen assertion that "Voith discloses that efficiency in the use of memory is desirable." On this point, I disagree with Dr. Jacobsen for the reasons set forth at ¶ 379 *supra.*

385. With reference to the G.993.1 standard, Dr. Jacobsen asserts that "G.993.1 discloses how memory is allocated in accordance with a message received during initialization" and that "[o]ne of ordinary skill in the art would therefore have recognized that the teachings of G.993.1 show a reliable and efficient way of enabling the transceivers of Mazzoni to partition the shared memory between the interleaver and deinterleaver without requiring all of the possible services to be defined in advance to create the table disclosed in Mazzoni." Jacobsen Report at ¶ 627. I disagree, there is no disclosure or suggestion in G.993.1 of using or partitioning shared memory. Dr. Jacobsen does not cite any portion of G.993.1 as purportedly disclosing this. On the contrary, a POSITA would understand G.993.1 to provide for dedicated downstream memories in each transceiver and separate, dedicated upstream memories in each transceiver. The use of such dedicated memories is consistent with other DSL modems of that era and proposals for VDSL modems, including the LB-031 modem. *See* §§ IV and VI.A.5.a.ii, *supra*. As explained in these cited sections above, portions of dedicated

interleaver memory that are not needed for interleaving cannot be allocated for use by the deinterleaver, and vice versa. Instead, those portions simply go unused. *Id.*

386. Further, a POSITA would not look to add messages (from G.993.1 or otherwise) to the system disclosed in Mazzoni, and in fact doing so would provide no useful benefit. It would certainly not be any more reliable and efficient than Mazzoni's existing scheme. This is because the system disclosed in Mazzoni relies on the use of a pre-populated table of I, M, I', and M' parameter values, where each set of values corresponds to a respective one of a number of predetermined data rate service pairs. *See* Mazzoni at 5:22-23, 5:27-30, 6:51-55. There is no use for a message that specifies the interleaver or deinterleaver memory sizes because all data rate pairs and their corresponding I, M, I', and M' values that need to be supported are accounted for. Mazzoni contemplates TO and TU transceiver pairs that will both be efficiently and reliably preconfigured at the time of installation with the same predetermined parameters selected from a limited number of possibilities. Thus, exchanging messages describing the capabilities of the transceivers would be redundant, serve no useful purpose, and make the system less reliable and efficient.

387. Therefore, it is my opinion that a POSITA would not have been motivated to combine Mazzoni with Voith and G.993.1 in the manner proposed by Dr. Jacobsen, and Dr. Jacobsen has not shown otherwise.

VII. CONCLUSION

388. For the foregoing reasons, it is my opinion that the Asserted Claims of the Family 3 Patent are valid and are neither anticipated nor obvious in view of the prior art and the knowledge of a person of ordinary skill in the art.

EXHIBIT 1

MATERIALS REVIEWED

Case-related filings

September 6, 2017 Parties' Joint Claim Construction Brief for the Family 3 Patents (Doc 353)

December 18, 2017 Claim Construction Memorandum Opinion – Family 3

December 28, 2017 Claim Construction Order for Family 3 Patents

January 30, 2018 Claim Construction Memorandum Opinion – Family 1

February 6, 2018 Claim Construction Order for Family 1 Patents

November 28, 2018 Opening Expert Report on Invalidity of Dr. Krista S. Jacobsen for Family 3 Patents and Cited Materials

Patents

US Patent No. 7,836,381 (TQD000221 – TQD000232)

File History for US Patent No. 7,836,381 (TQD003999 – TQD004178)

US Patent No. 7,844,882 (TQD000233 – TQD000244)

File History for US Patent No. 7,844,882 (TQD004179 – TQD004385)

US Patent No. 8,276,048 (TQD000345 – TQD000356)

File History for US Patent No. 8,276,048 (TQD008758 – TQD009818)

US Patent No. 8,495,473 (TQD000486 – TQD000498)

File History for US Patent No. 8,495,473 (TQD016048 – TQD017127)

Standards

Document name	Bates number
ITU-T G.993.2 - Very high speed digital subscriber line transceivers 2 (VDSL2), 12/2011	TQD114647 - TQD115022
Original ADSL standard, T1.413 Issue 1 (also referred to as T1.413-1995)	2WIRE00029898 – 2WIRE00030083
T1.413 Issue 2 (also referred to as T1.413-1998)	2WIRE00029628 – 2WIRE00029897
ITU-T Recommendation G.992.1 (also referred to as "ADSL1")	2WIRE00029369 – 2WIRE00029624

ITU-T Recommendation G.992.2 (also referred to as "G.lite")	2WIRE00052246 – 2WIRE00052424
ITU-T Recommendation G.992.3 (also referred to as "ADSL2")	2WIRE00030376 - 2WIRE00030687
ITU-T Recommendation G.992.5 (also referred to as "ADSL2+")	TQD078348 – TQD078439
ITU-T Recommendation, G.993.1	2WIRE00030729 – 2WIRE00030956
SG15/Q4 June 2004 (Leuven, Belgium) Document List (LB-000.txt, which lists the contributions to the Leuven meeting, including LB-031)	2WIRE00054590 – 2WIRE00054608
LB-U11R4	2WIRE00054698 – 2WIRE00054713
LB-U11	2WIRE00054672 – 2WIRE00054696
ITU-T SG/15/Q4 Contribution LB-031 ("LB-031"), entitled "VDSL2 – Constraining the Interleaver Complexity	2WIRE00030957 – 2WIRE00030963
Temporary Document LB-004 (00_doc_list.html, which was generated on June 16, 2004 by Steve Palm)	2WIRE00054667 – 2WIRE00054671